JEDEC STANDARD

Addendum No. 1 to JESD209-4 - Low Power Double Data Rate 4X (LPDDR4X)

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(From JEDEC Board Ballot JCB-16-49, formulated under the cognizance of the JC-42.6 Subcommittee on Low Power Memories.)

1 Scope

This document defines the LPDDR4 standard, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this specification is to define the minimum set of requirements for a JEDEC compliant 16 bit per channel SDRAM device with either one or two channels. LPDDR4 dual channel device density ranges from 4 Gb through 32 Gb and single channel density ranges from 2 Gb through 16 Gb. This document was created using aspects of the following standards: DDR2 (JESD79-2), DDR3 (JESD79-3), DDR4 (JESD79-4), LPDDR (JESD209), LPDDR2 (JESD209-2) and LPDDR3 (JESD209-3).

Each aspect of the standard was considered and approved by committee ballot(s). The accumulation of these ballots was then incorporated to prepare the LPDDR4 standard.

This addendum defines LPDDR4X specifications that supersede the LPDDR4 Standard (JESD209-4) to enable low V_{DDQ} operation of LPDDR4X devices to reduce power consumption.

2 Package Ballout and Pin Definition

2.1 Pad Order

Ch. A Top	
1	VDD2
2	VSS
3	VDD1
4	VDD2
5	VSS
6	VSSQ
7	DQ8_A
8	VDDQ
9	DQ9_A
10	VSSQ
11	DQ10_A
12	VDDQ
13	DQ11_A
14	VSSQ
15	DQS1_t_A
16	DQS1_c_A
17	VDDQ
18	DMI1_A
19	VSSQ
20	DQ12_A
21	VDDQ
22	DQ13_A
23	VSSQ
24	DQ14_A
25	VDDQ
26	DQ15_A
27	VSSQ
28	ZQ
29	VDDQ
30	VDD2
31	VDD1
32	VSS
33	CA5_A
34	CA4_A
35	VDD2
36	CA3_A
37	CA2_A
38	VSS
39	CK_c_A
40	CK_t_A
Ch. A Top	

41	VDD2
42	CKE_A
43	CS_A
44	VSS
45	CA1_A
46	CA0_A
47	VDD2
48	ODT(ca)_A
49	VSS
50	VDD1
51	VSSQ
52	DQ7_A
53	VDDQ
54	DQ6_A
55	VSSQ
56	DQ5_A
57	VDDQ
58	DQ4_A
59	VSSQ
60	DMI0_A
61	VDDQ
62	DQS0_c_A
63	DQS0_t_A
64	VSSQ
65	DQ3_A
66	VDDQ
67	DQ2_A
68	VSSQ
69	DQ1_A
70	VDDQ
71	DQ0_A
72	VSSQ
73	VSS
74	VDD2
75	VDD1
76	VSS
77	VDD2
Ch. A Bottom	

Ch. B Top	
101	VDD2
102	VSS
103	VDD1
104	VDD2
105	VSS
106	VSSQ
107	DQ8_B
108	VDDQ
109	DQ9_B
110	VSSQ
111	DQ10_B
112	VDDQ
113	DQ11_B
114	VSSQ
115	DQS1_t_B
116	DQS1_c_B
117	VDDQ
118	DMI1_B
119	VSSQ
120	DQ12_B
121	VDDQ
122	DQ13_B
123	VSSQ
124	DQ14_B
125	VDDQ
126	DQ15_B
127	VSSQ
128	RESET_n
129	VDDQ
130	VDD2
131	VDD1
132	VSS
133	CA5_B
134	CA4_B
135	VDD2
136	CA3_B
137	CA2_B
138	VSS
139	CK_c_B
140	CK_t_B
Ch. B Top	

141	VDD2
142	CKE_B
143	CS_B
144	VSS
145	CA1_B
146	CA0_B
147	VDD2
148	ODT(ca)_B
149	VSS
150	VDD1
151	VSSQ
152	DQ7_B
153	VDDQ
154	DQ6_B
155	VSSQ
156	DQ5_B
153	VDDQ
158	DQ4_B
159	VSSQ
160	DMI0_B
161	VDDQ
162	DQS0_c_B
163	DQS0_t_B
164	VSSQ
165	DQ3_B
166	VDDQ
167	DQ2_B
168	VSSQ
169	DQ1_B
170	VDDQ
171	DQ0_B
172	VSSQ
173	VSS
174	VDD2
175	VDD1
176	VSS
177	VDD2
Ch. B Bottom	

NOTE 1 Applications are recommended to follow bit/byte assignments. Bit or Byte swapping at the application level requires review of MR and calibration features assigned to specific data bits/bytes.

NOTE 2 Additional pads are allowed for DRAM mfg-specific pads (“DNU”), or additional power pads as long as the extra pads are grouped with like-named pads.

NOTE 3 V_{DDQ} pads ((#12,#21,#57,#66,#112,#121,#157 and #166) may be individually assigned to either V_{DDQ} or V_{DD2}. Please refer to vendor specification.

2.2 Single Channel Pad Order

Top	
1	VDD2
2	VSS
3	VDD1
4	VDD2
5	VSS
6	VSSQ
7	DQ8
8	VDDQ
9	DQ9
10	VSSQ
11	DQ10
12	VDDQ
13	DQ11
14	VSSQ
15	DQS1_t
16	DQS1_c
17	VDDQ
18	DMI1
19	VSSQ
20	DQ12
21	VDDQ
22	DQ13
23	VSSQ
24	DQ14
25	VDDQ
26	DQ15
27	VSSQ
28	ZQ
29	VDDQ
30	VDD2
31	RESET_n
32	VDD1
33	VSS
34	CA5
35	CA4
36	VDD2
37	CA3
38	CA2
39	VSS

40	CK_c
41	CK_t
42	VDD2
43	CKE
44	CS
45	VSS
46	CA1
47	CA0
48	VDD2
49	ODT(ca)
50	VSS
51	VDD1
52	VSSQ
53	DQ7
54	VDDQ
55	DQ6
56	VSSQ
57	DQ5
58	VDDQ
59	DQ4
60	VSSQ
61	DMI0
62	VDDQ
63	DQS0_c
64	DQS0_t
65	VSSQ
66	DQ3
67	VDDQ
68	DQ2
69	VSSQ
70	DQ1
71	VDDQ
72	DQ0
73	VSSQ
74	VSS
75	VDD2
76	VDD1
77	VSS
78	VDD2
Bottom	

NOTE 1 Applications are recommended to follow bit/byte assignments. Bit or Byte swapping at the application level requires review of MR and calibration features assigned to specific data bits/bytes.

NOTE 2 Additional pads are allowed for DRAM mfg-specific pads (“DNU”), or additional power pads as long as the extra pads are grouped with like-named pads.

NOTE 3 V_{DDQ} pads (#12, #21, #57 and #66) may be individually assigned to either V_{DDQ} or V_{DD2}. Please refer to vendor specification.

NOTE 4 A RESET_n pad is added. The RESET_n pad location is vendor specific. See vendor device datasheets for details about RESET_n pad location.