JEDEC STANDARD

Addendum No. 1 to JESD79-4, 3D Stacked DRAM

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(From JEDEC Board Ballot JCB-16-29, formulated under the cognizance of the JC-42.3C Subcommittee on DRAM Parametrics.)

1 Scope

This document defines the 3DS DDR4 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this specification is to define the minimum set of requirements for a compliant 8 Gbit through 128 Gbit for x4, x8 3DS DDR4 SDRAM devices. This addendum was created based on the JESD79-4 DDR4 SDRAM specification. Each aspect of the changes for 3DS DDR4 SDRAM operation was considered. Any TBD's, as of the publication of this document, are under discussion by the formulating committee.

The requirement for 3DS devices compliant to this spec addendum is to have a single electrical load for the stacked devices no matter if the stack is comprised of 2, 4 or 8 devices. The I/O buffer circuitry can be built into the base SDRAM of the stack or into a separate logic buffer device. In either case (built in native circuitry or separate logic die), the assumption is that the I/O buffers are located at the bottom of the stack closest to the package substrate. All pictures and diagrams in the spec depict a master die at the bottom of the stack; it is associated with logical rank 0.

2 3DS SDRAM Package Pinout and Addressing

2.1 Overview

These ballouts have been derived from JESD79-4. The ballout comprehends x4 and x8 data widths, where x4 is a subset of the x8 ballout, and the addressing described in this section.

2.2 Pinout Description

The following table only documents differences of DDR4 3DS SDRAMs relative to the pinout description in JESD79-4.

Symbol	Type	Function
PAR	Input	Command and Address Parity Input : DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,BG0-BG1,BA0-BA1,A17-A0 and C0, C1, C2. Input parity should maintain at the rising edge of the clock and at the same time with command and address with CS_n LOW
NOTE 1 Input only pins (BG0-BG1,BA0-BA1, A0-A17, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, C0, C1, C2 and RESET_n) do not supply termination.		

2.3 3D Stacked / DDR4 SDRAM x4 Ballout using MO-207

Ball locations in Figure 1, "3D Stacked DDR4 SDRAM x4 Ballout" show the proposed DDR4 3D Stacked SDRAM x4 ballout.

[X-ray view from package top surface]

	1	2	3	4	5	6	7	8	9	
	NC		NC				NC		NC	NC
	NC		NC				NC		NC	NC
A	VDD	VSSQ	NC				NC	VSSQ	VSS	NC
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	
D	VSSQ	NC	DQ2				DQ3	NC	VSSQ	
E	VSS	VDDQ	NC				NC	VDDQ	VSS	
F	VDD	C2, NC[1]	ODT				CK_t	CK_c	VDD	
G	VSS	C0	CKE				CS_n	C1, NC[2]	RFU	
H	VDD	WE_n, A14	ACT_n				CAS_n, A15	RAS_n, A16	VSS	
J	VREFCA	BG0	A10, AP				A12, BC_n	BG1	VDD	
K	VSS	BA0	A4				A3	BA1	VSS	
L	RESET_n	A6	A0				A1	A5	ALERT_n	
M	VDD	A8	A2				A9	A7	VPP	
N	VSS	A11	PAR				A17, NC[3],	A13	VDD	NC
	NC		NC				NC		NC	NC
	NC		NC				NC		NC	NC

1.This pin is not connected for 3DS devices with two or four logical ranks.
2.This pin is not connected for 3DS devices with two logical ranks.
3.This pin is not connected for 4Gb and 8Gb devices.

Figure 1 — 3D Stacked DDR4 SDRAM x4 Ballout