

IEEE Standard for Ethernet

Amendment 10: Media Access Control Parameters, Physical Layers, and Management Parameters for 200 Gb/s and 400 Gb/s Operation

IEEE Computer Society

Sponsored by the
LAN/MAN Standards Committee

IEEE
3 Park Avenue
New York, NY 10016-5997
USA

IEEE Std 802.3bs™-2017
(Amendment to
IEEE Std 802.3™-2015
as amended by
IEEE Std 802.3bw™-2015,
IEEE Std 802.3by™-2016,
IEEE Std 802.3bq™-2016,
IEEE Std 802.3bp™-2016,
IEEE Std 802.3br™-2016,
IEEE Std 802.3bn™-2016,
IEEE Std 802.3bz™-2016,
IEEE Std 802.3bu™-2016,
IEEE Std 802.3bv™-2017, and
IEEE Std 802.3-2015/Cor 1-2017)

IEEE Std 802.3bs™-2017

(Amendment to
IEEE Std 802.3™-2015
as amended by
IEEE Std 802.3bw™-2015,
IEEE Std 802.3by™-2016,
IEEE Std 802.3bq™-2016,
IEEE Std 802.3bp™-2016,
IEEE Std 802.3br™-2016,
IEEE Std 802.3bn™-2016,
IEEE Std 802.3bz™-2016,
IEEE Std 802.3bu™-2016,
IEEE Std 802.3bv™-2017, and
IEEE Std 802.3-2015/Cor 1-2017)

IEEE Standard for Ethernet

Amendment 10: Media Access Control Parameters, Physical Layers, and Management Parameters for 200 Gb/s and 400 Gb/s Operation

**LAN/MAN Standards Committee
of the
IEEE Computer Society**

**Approved 6 December 2017
of the
IEEE-SA Standards Board**

Abstract: Clause 116 through Clause 124 and Annex 119A through Annex 120E are added by this amendment to IEEE Std 802.3-2015. This amendment includes IEEE 802.3 Media Access Control (MAC) parameters, Physical Layer specifications, and management parameters for the transfer of IEEE 802.3 format frames at 200 Gb/s and 400 Gb/s.

Keywords: 200 Gb/s Ethernet, 200GAUI-4, 200GAUI-8, 200GBASE-DR4, 200GBASE-FR4, 200GBASE-LR4, 200GBASE-R, 200GMII, 200GXS, 400 Gb/s Ethernet, 400GAUI-8, 400GAUI-16, 400GBASE-DR4, 400GBASE-FR8, 400GBASE-LR8, 400GBASE-SR16, 400GBASE-R, 400GMII, 400GXS, EEE, Energy Efficient Ethernet, Ethernet, FEC, forward error correction, IEEE 802.3™, IEEE 802.3bs™, MMF, PAM4, Physical Medium Dependent sublayer, PMD, SMF

The Institute of Electrical and Electronics Engineers, Inc.
3 Park Avenue, New York, NY 10016-5997, USA

Copyright © 2017 by The Institute of Electrical and Electronics Engineers, Inc.
All rights reserved. Published 12 December 2017. Printed in the United States of America.

IEEE and 802 are registered trademarks in the U.S. Patent & Trademark Office, owned by The Institute of Electrical and Electronics Engineers, Incorporated.

PDF: ISBN 978-1-5044-4450-7 STD22871
Print: ISBN 978-1-5044-4451-4 STDPD22871

IEEE prohibits discrimination, harassment and bullying. For more information, visit <http://www.ieee.org/web/aboutus/whatis/policies/p9-26.html>.

No part of this publication may be reproduced in any form, in an electronic retrieval system or otherwise, without the prior written permission of the publisher.

Important Notices and Disclaimers Concerning IEEE Standards Documents

IEEE documents are made available for use subject to important notices and legal disclaimers. These notices and disclaimers, or a reference to this page, appear in all standards and may be found under the heading “Important Notices and Disclaimers Concerning IEEE Standards Documents.” They can also be obtained on request from IEEE or viewed at <http://standards.ieee.org/IPR/disclaimers.html>.

Notice and Disclaimer of Liability Concerning the Use of IEEE Standards Documents

IEEE Standards documents (standards, recommended practices, and guides), both full-use and trial-use, are developed within IEEE Societies and the Standards Coordinating Committees of the IEEE Standards Association (“IEEE-SA”) Standards Board. IEEE (“the Institute”) develops its standards through a consensus development process, approved by the American National Standards Institute (“ANSI”), which brings together volunteers representing varied viewpoints and interests to achieve the final product. IEEE Standards are documents developed through scientific, academic, and industry-based technical working groups. Volunteers in IEEE working groups are not necessarily members of the Institute and participate without compensation from IEEE. While IEEE administers the process and establishes rules to promote fairness in the consensus development process, IEEE does not independently evaluate, test, or verify the accuracy of any of the information or the soundness of any judgments contained in its standards.

IEEE Standards do not guarantee or ensure safety, security, health, or environmental protection, or ensure against interference with or from other devices or networks. Implementers and users of IEEE Standards documents are responsible for determining and complying with all appropriate safety, security, environmental, health, and interference protection practices and all applicable laws and regulations.

IEEE does not warrant or represent the accuracy or content of the material contained in its standards, and expressly disclaims all warranties (express, implied and statutory) not included in this or any other document relating to the standard, including, but not limited to, the warranties of: merchantability; fitness for a particular purpose; non-infringement; and quality, accuracy, effectiveness, currency, or completeness of material. In addition, IEEE disclaims any and all conditions relating to: results; and workmanlike effort. IEEE standards documents are supplied “AS IS” and “WITH ALL FAULTS.”

Use of an IEEE standard is wholly voluntary. The existence of an IEEE standard does not imply that there are no other ways to produce, test, measure, purchase, market, or provide other goods and services related to the scope of the IEEE standard. Furthermore, the viewpoint expressed at the time a standard is approved and issued is subject to change brought about through developments in the state of the art and comments received from users of the standard.

In publishing and making its standards available, IEEE is not suggesting or rendering professional or other services for, or on behalf of, any person or entity nor is IEEE undertaking to perform any duty owed by any other person or entity to another. Any person utilizing any IEEE Standards document, should rely upon his or her own independent judgment in the exercise of reasonable care in any given circumstances or, as appropriate, seek the advice of a competent professional in determining the appropriateness of a given IEEE standard.

IN NO EVENT SHALL IEEE BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO: PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE PUBLICATION, USE OF, OR RELIANCE UPON ANY STANDARD, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE AND REGARDLESS OF WHETHER SUCH DAMAGE WAS FORESEEABLE.

Translations

The IEEE consensus development process involves the review of documents in English only. In the event that an IEEE standard is translated, only the English version published by IEEE should be considered the approved IEEE standard.

Official statements

A statement, written or oral, that is not processed in accordance with the IEEE-SA Standards Board Operations Manual shall not be considered or inferred to be the official position of IEEE or any of its committees and shall not be considered to be, or be relied upon as, a formal position of IEEE. At lectures, symposia, seminars, or educational courses, an individual presenting information on IEEE standards shall make it clear that his or her views should be considered the personal views of that individual rather than the formal position of IEEE.

Comments on standards

Comments for revision of IEEE Standards documents are welcome from any interested party, regardless of membership affiliation with IEEE. However, IEEE does not provide consulting information or advice pertaining to IEEE Standards documents. Suggestions for changes in documents should be in the form of a proposed change of text, together with appropriate supporting comments. Since IEEE standards represent a consensus of concerned interests, it is important that any responses to comments and questions also receive the concurrence of a balance of interests. For this reason, IEEE and the members of its societies and Standards Coordinating Committees are not able to provide an instant response to comments or questions except in those cases where the matter has previously been addressed. For the same reason, IEEE does not respond to interpretation requests. Any person who would like to participate in revisions to an IEEE standard is welcome to join the relevant IEEE working group.

Comments on standards should be submitted to the following address:

Secretary, IEEE-SA Standards Board
445 Hoes Lane
Piscataway, NJ 08854 USA

Laws and regulations

Users of IEEE Standards documents should consult all applicable laws and regulations. Compliance with the provisions of any IEEE Standards document does not imply compliance to any applicable regulatory requirements. Implementers of the standard are responsible for observing or referring to the applicable regulatory requirements. IEEE does not, by the publication of its standards, intend to urge action that is not in compliance with applicable laws, and these documents may not be construed as doing so.

Copyrights

IEEE draft and approved standards are copyrighted by IEEE under U.S. and international copyright laws. They are made available by IEEE and are adopted for a wide variety of both public and private uses. These include both use, by reference, in laws and regulations, and use in private self-regulation, standardization, and the promotion of engineering practices and methods. By making these documents available for use and adoption by public authorities and private users, IEEE does not waive any rights in copyright to the documents.

Photocopies

Subject to payment of the appropriate fee, IEEE will grant users a limited, non-exclusive license to photocopy portions of any individual standard for company or organizational internal use or individual, non-commercial use only. To arrange for payment of licensing fees, please contact Copyright Clearance Center, Customer Service, 222 Rosewood Drive, Danvers, MA 01923 USA; +1 978 750 8400. Permission to photocopy portions of any individual standard for educational classroom use can also be obtained through the Copyright Clearance Center.

Updating of IEEE Standards documents

Users of IEEE Standards documents should be aware that these documents may be superseded at any time by the issuance of new editions or may be amended from time to time through the issuance of amendments, corrigenda, or errata. An official IEEE document at any point in time consists of the current edition of the document together with any amendments, corrigenda, or errata then in effect.

Every IEEE standard is subjected to review at least every ten years. When a document is more than ten years old and has not undergone a revision process, it is reasonable to conclude that its contents, although still of some value, do not wholly reflect the present state of the art. Users are cautioned to check to determine that they have the latest edition of any IEEE standard.

In order to determine whether a given document is the current edition and whether it has been amended through the issuance of amendments, corrigenda, or errata, visit the IEEE Xplore at <http://ieeexplore.ieee.org/> or contact IEEE at the address listed previously. For more information about the IEEE-SA or IEEE's standards development process, visit the IEEE-SA Website at <http://standards.ieee.org>.

Errata

Errata, if any, for all IEEE standards can be accessed on the IEEE-SA Website at the following URL: <http://standards.ieee.org/findstds/errata/index.html>. Users are encouraged to check this URL for errata periodically.

Patents

Attention is called to the possibility that implementation of this standard may require use of subject matter covered by patent rights. By publication of this standard, no position is taken by the IEEE with respect to the existence or validity of any patent rights in connection therewith. If a patent holder or patent applicant has filed a statement of assurance via an Accepted Letter of Assurance, then the statement is listed on the IEEE-SA Website at <http://standards.ieee.org/about/sasb/patcom/patents.html>. Letters of Assurance may indicate whether the Submitter is willing or unwilling to grant licenses under patent rights without compensation or under reasonable rates, with reasonable terms and conditions that are demonstrably free of any unfair discrimination to applicants desiring to obtain such licenses.

Essential Patent Claims may exist for which a Letter of Assurance has not been received. The IEEE is not responsible for identifying Essential Patent Claims for which a license may be required, for conducting inquiries into the legal validity or scope of Patents Claims, or determining whether any licensing terms or conditions provided in connection with submission of a Letter of Assurance, if any, or in any licensing agreements are reasonable or non-discriminatory. Users of this standard are expressly advised that determination of the validity of any patent rights, and the risk of infringement of such rights, is entirely their own responsibility. Further information may be obtained from the IEEE Standards Association.

Participants

The following individuals were officers and members of the IEEE 802.3 working group at the beginning of the IEEE P802.3bs working group ballot. Individuals may have not voted or may have voted for approval, disapproval, or abstention on this amendment.

David J. Law, *IEEE 802.3 Working Group Chair*
Adam Healey, *IEEE 802.3 Working Group Vice-Chair*
Pete Anslow, *IEEE 802.3 Working Group Secretary*
Steven B. Carlson, *IEEE 802.3 Working Group Executive Secretary*
Valerie Maguire, *IEEE 802.3 Working Group Treasurer*

John D'Ambrosia, *IEEE P802.3bs 200 Gb/s and 400 Gb/s Ethernet Task Force Chair*
Pete Anslow, *IEEE P802.3bs 200 Gb/s and 400 Gb/s Ethernet Task Force Editor-in-Chief*
Mark Gustlin, *IEEE P802.3bs 200 Gb/s and 400 Gb/s Ethernet Task Force Editor for Clauses 117, 118, 119, Annex 119A*
Steve Trowbridge, *IEEE P802.3bs 200 Gb/s and 400 Gb/s Ethernet Task Force Editor for Clause 120, Annex 120A*
Peter Stassar, *IEEE P802.3bs 200 Gb/s and 400 Gb/s Ethernet Task Force Editor for Clauses 121, 122, 124*
Jonathan King,¹ *IEEE P802.3bs 200 Gb/s and 400 Gb/s Ethernet Task Force Editor for Clause 123*
Andre Szczepanek, *IEEE P802.3bs 200 Gb/s and 400 Gb/s Ethernet Task Force Editor for Annexes 120D, 120E*

Justin Abbott	David Chalupsky	Andrew Gardner
David Abramson	Jacky Chang	Claude Gauthier
Shadi Abughazaleh	Xin Chang	Ali Ghiasi
Mohammad Ahmed	Ahmad Chini	Joel Goergen
Eric Baden	Keng Hua Chuang	Volker Goetzfried
Amrik Bains	Christopher R. Cole	Zhigang Gong
Thananya Baldwin	Yair Darshan	Steven Gorshe
Denis Beaudoin	Piers Dawe	Robert Grow
Christian Beia	Fred Dawson	Marek Hajduczenia
Michael Bennett	Wael Diab	Takehiro Hayashi
Vipul Bhatt	Eric DiBioso	Yasuo Hidaka
William Bliss	John Dillard	Rita Horner
Brad Booth	Daniel Dillow	Bernd Horrmeyer
Martin Bouda	Thuyen Dinh	Victor Hou
Ralf-Peter Braun	Curtis Donahue	Yasuhiro Hyakutake
Theodore Brillhart	Dan Dove	Hideki Isono
Paul Brooks	Mike Dudek	Tom Issenhuth
Alan Brown	David Dwelley	Kenneth Jackson
Matthew Brown	Frank Effenberger	Andrew Jimenez
Chris Bullock	Hesham Elbakoury	Chad Jones
Jairo Bustos Heredia	David Estes	Peter Jones
Adrian Butter	John Ewen	Manabu Kagami
Francesco Caggioni	Ramin Farjad	Upen Kareti
Anthony Calbone	Shahar Feldman	Keisuke Kawahara
Clark Carty	James Fife	Yasuaki Kawatsu
Craig Chabot	Alan Flatman	Michael Kelsen
Geoffrey Chacon Simon	Matthias Fritsche	Scott Kipp
Mandeep Chadha	Richard Frosch	Michael Klempa

¹Not a member of the IEEE 802.3 working group at the beginning of the working group ballot.

Curtis Knittle
Shigeru Kobayashi
Daniel Koehler
Paul Kolesar
Tom Kolze
Glen Kramer
Hans Lackner
Jeffrey Lapak
Mark Laubach
Han Hyub Lee
David Lewis
Jon Lewis
Mike Peng Li
Jane Lim
Dekun Liu
Hai-Feng Liu
William Lo
Miklos Lukacs
Kent Lusted
Jeffery Maki
David Malicoat
Yonatan Malkiman
Arthur Marris
Takeo Masuda
Erdem Matoglu
Naoki Matsuda
Mick McCarthy
Brett McClellan
Thomas McDermott
John McDonough
Larry McMillan
Richard Mei
Richard Mellitz
Bryan Moffitt
Ardeshir Mohammadian
Paul Mooney
Dale Murray
Henry Muyshondt
James Nadolny

Edward Nakamoto
Gary Nicholl
Kevin Noll
Mark Nowell
David Ofelt
Tom Palkert
Hui Pan
Sesha Panguluri
Vasu Parthasarathy
Petar Pepeljugoski
Gerald Pepper
Ruben Perez De Aranda Alonso
Michael Peters
Phong Pham
Jean Picard
William Powell
Rick Rabinovich
Adee Ran
Alon Regev
Duane Remein
Victor Renteria
Christopher Roth
Salvatore Rotolo
Toshiaki Sakai
Jorge Salinger
Sam Sambasivan
Edward Sayre
Dieter Schicketanz
Fred Schindler
Hossein Sedarat
Naoshi Serizawa
Masood Shariff
Ramin Shirani
Tom Skaar
Jeff Slavick
Daniel Smith
Scott Sommers
Yoshiaki Sone
Tom Souvignier
Heath Stewart

Robert Stone
David Stover
Junqing Sun
Ken-Ichi Suzuki
Steve Swanson
William Szeto
Bharat Tailor
Takayuki Tajima
Satoshi Takahashi
Kohichi Tamura
Brian Teipen
Geoffrey Thompson
Pirooz Tooyserkani
Albert Tretter
Yoshihiro Tsukamoto
Ed Ulrichs
Alexander Umnov
Sterling A. Vaden
Stefano Valle
Paul Vanderlaan
Robert Wagner
Dylan Walker
Haifei Wang
Roy Wang
Tongtong Wang
Xinyuan Wang
Matthias Wendt
Oded Wertheim
Natalie Wienckowski
Ludwig Winkel
Peter Wu
Dayin Xu
Yu Xu
Jun Yi
Lennart Yseboodt
Hayato Yuki
Andrew Zambell
Yan Zhuang
George Zimmerman

The following members of the individual balloting committee voted on this amendment. Balloters may have voted for approval, disapproval, or abstention.

Mohammad Ahmed	Werner Hoelzl	Glenn Parsons
Thomas Alexander	Rita Horner	Bansi Patel
Pete Anslow	Noriyuki Ikeuchi	Arumugam Paventhan
Butch Anton	Sergiu Iordanescu	Michael Peters
Stefan Aust	Osamu Ishida	David Piehler
Eric Baden	Atsushi Ito	Rick Pimpinella
Saman Behtash	Raj Jain	Adee Ran
Ralf-Peter Braun	SangKwon Jeong	Alon Regev
Nancy Bravin	Piotr Karocki	Maximilian Riegel
Theodore Brillhart	Stuart Kerry	Robert Robinson
Matthew Brown	Yongbum Kim	Toshiaki Sakai
Jairo Bustos Heredia	Jonathan King	Osman Sakr
William Byrd	Paul Kolesar	Dieter Schicketanz
Steven B. Carlson	Mark Laubach	Takeshi Shimizu
Juan Carreon	David J. Law	Kapil Shrikhande
David Chalupsky	June Hee Lee	Jeff Slavick
Boung Wook Cho	David Lewis	Thomas Starai
Keith Chow	Jon Lewis	Peter Stassar
Keng Hua Chuang	Mike-Peng Li	Rene Struik
Charles Cook	Arthur H. Light	Walter Struppler
Eugene Dai	Kent Lusted	Mitsutoshi Sugawara
John D'Ambrosia	Elvis Maculuba	Patrik Sundstrom
Piers J. G. Dawe	Valerie Maguire	James Theodoras
Patrick Diamond	Jeffery Maki	David Thompson
Michael Dudek	Arthur Marris	Geoffrey Thompson
John French	Mick McCarthy	Michael Thompson
Matthias Fritsche	Brett McClellan	Steven Tilden
Yukihiro Fujimoto	Thomas McDermott	Steve Trowbridge
Ali Ghiasi	Michael McInnis	Mark-Rene Uchida
Joel Goergen	Richard Mellitz	Alexander Umnov
Zhigang Gong	Tremont Miao	Paul Vanderlaan
James Graba	Jeffrey Moore	Dmitri Varsanofiev
Randall Groves	Charles Moorwood	George Vlantis
Robert Grow	Jose Morales	Khurram Waheed
Mark Gustlin	Michael Newman	Oded Wertheim
Adam Healey	Nick S. A. Nikjoo	Andreas Wolf
Marco Hernandez	Paul Nikolich	Peter Wu
David Hess	Mark Nowell	Jun Xu
Yasuo Hidaka	Satoshi Obara	Oren Yuen
Guido Hiertz	Thomas Palkert	Zhen Zhou

When the IEEE-SA Standards Board approved this amendment on 6 December 2017, it had the following membership:

Jean-Philippe Faure, *Chair*
Gary Hoffman, *Vice Chair*
John D. Kulick, *Past Chair*
Konstantinos Karachalios, *Secretary*

Chuck Adams	Thomas Kochy	Robby Robson
Masayuki Ariyoshi	Joseph L. Koepfinger*	Dorothy Stanley
Ted Burse	Kevin Lu	Adrian Stephens
Stephen Dukes	Daleep Mohla	Mehmet Ulema
Doug Edwards	Damir Novosel	Phil Wennblom
J. Travis Griffith	Ronald C. Petersen	Howard Wolfman
Michael Janezic	Annette D. Reilly	Yu Yuan

*Member Emeritus

Introduction

This introduction is not part of IEEE Std 802.3bs-2017, IEEE Standard for Ethernet—Amendment 10: Media Access Control Parameters, Physical Layers, and Management Parameters for 200 Gb/s and 400 Gb/s Operation.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2015 and are not maintained as separate documents.

At the publication date of IEEE Std 802.3bs-2017, IEEE Std 802.3 is composed of the following documents:

IEEE Std 802.3-2015

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between

stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes includes general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

IEEE Std 802.3bw™-2015

Amendment 1—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 96. This amendment adds 100 Mb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable.

IEEE Std 802.3by™-2016

Amendment 2—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 105 through Clause 112, Annex 109A, Annex 109B, Annex 109C, Annex 110A, Annex 110B, and Annex 110C. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 25 Gb/s.

IEEE Std 802.3bq™-2016

Amendment 3—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 113 and Annex 113A. This amendment adds new Physical Layers for 25 Gb/s and 40 Gb/s operation over balanced twisted-pair structured cabling systems.

IEEE Std 802.3bp™-2016

Amendment 4—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 97 and Clause 98. This amendment adds point-to-point 1 Gb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable in automotive and other applications not utilizing the structured wiring plant.

IEEE Std 802.3br™-2016

Amendment 5—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 99. This amendment adds a MAC Merge sublayer and a MAC Merge Service Interface to support for Interspersing Express Traffic over a single link.

IEEE Std 802.3bn™-2016

Amendment 6—This amendment adds the Physical Layer specifications and management parameters for symmetric and/or asymmetric operation of up to 10 Gb/s on point-to-multipoint Radio Frequency (RF) distribution plants comprising either amplified or passive coaxial media. It also extends the operation of Ethernet Passive Optical Networks (EPON) protocols, such as Multipoint Control Protocol (MPCP) and Operation Administration and Management (OAM).

IEEE Std 802.3bz™-2016

Amendment 7—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 125 and Clause 126. This amendment adds new rates of 2.5 Gb/s and 5 Gb/s and new Physical Layers for operation at 2.5 Gb/s and 5 Gb/s over balanced twisted-pair structured cabling systems.

IEEE Std 802.3bu™-2016

Amendment 8—This amendment includes changes to IEEE Std 802.3-2015 to define a methodology for the provision of power via a single twisted pair to connected Data Terminal Equipment (DTE) with IEEE 802.3 single twisted-pair interfaces.

IEEE Std 802.3bv™-2017

Amendment 9—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 115 and Annex 115A. This amendment adds point-to-point 1000 Mb/s Physical Layer (PHY) specifications and management parameters for operation on duplex plastic optical fiber (POF) targeting use in automotive, industrial, home-network, and other applications.

IEEE Std 802.3™-2015/Cor 1-2017

This corrigendum clarifies which lane of the media dependent interface (MDI) of a multi-lane Physical Layer entity (PHY) is used as the timestamping reference point.

IEEE Std 802.3bs™-2017

Amendment 10—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 116 through Clause 124 and Annex 119A through Annex 120E. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 200 Gb/s and 400 Gb/s.

A companion document IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of the enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

Contents

1. Introduction.....	31
1.1 Overview.....	31
1.1.3 Architectural perspectives.....	31
1.1.3.2 Compatibility interfaces.....	31
1.3 Normative references.....	32
1.4 Definitions.....	32
1.5 Abbreviations.....	34
4. Media Access Control.....	35
4.4 Specific implementations.....	35
4.4.2 MAC parameters.....	35
30. Management.....	36
30.2 Managed objects.....	36
30.2.5 Capabilities.....	36
30.3 Layer management for DTEs.....	36
30.3.2 PHY device managed object class.....	36
30.3.2.1 PHY device attributes.....	36
30.3.2.1.2 aPhyType.....	36
30.3.2.1.3 aPhyTypeList.....	37
30.3.2.1.5 aSymbolErrorDuringCarrier.....	37
30.5 Layer management for medium attachment units (MAUs).....	37
30.5.1 MAU managed object class.....	37
30.5.1.1 MAU attributes.....	37
30.5.1.1.2 aMAUType.....	37
30.5.1.1.4 aMediaAvailable.....	38
30.5.1.1.12 aLaneMapping.....	38
30.5.1.1.15 aFECAbility.....	38
30.5.1.1.17 aFECCorrectedBlocks.....	39
30.5.1.1.18 aFECUncorrectableBlocks.....	39
30.5.1.1.32 aPCSFECIndicationAbility.....	40
30.5.1.1.33 aPCSFECIndicationEnable.....	40
45. Management Data Input/Output (MDIO) Interface.....	41
45.2 MDIO Interface Registers.....	41
45.2.1 PMA/PMD registers.....	41
45.2.1.1 PMA/PMD control 1 register (Register 1.0).....	43
45.2.1.1.3 Speed selection (1.0.13, 1.0.6, 1.0.5:2).....	44
45.2.1.1.4 PMA remote loopback (1.0.1).....	44
45.2.1.1.5 PMA local loopback (1.0.0).....	44
45.2.1.2 PMA/PMD status 1 register (Register 1.1).....	44
45.2.1.2.3 Fault (1.1.7).....	44
45.2.1.4 PMA/PMD speed ability (Register 1.4).....	45
45.2.1.4.aaa 400G capable (1.4.15).....	45
45.2.1.4.ac 200G capable (1.4.12).....	45
45.2.1.6 PMA/PMD control 2 register (Register 1.7).....	45
45.2.1.6.3 PMA/PMD type selection (1.7.65:0).....	47
45.2.1.7 PMA/PMD status 2 register (Register 1.8).....	48

45.2.1.7.4	Transmit fault (1.8.11)	48
45.2.1.7.5	Receive fault (1.8.10)	48
45.2.1.8	PMD transmit disable register (Register 1.9)	48
45.2.1.8.1	PMD transmit disable 914 (1.9.1015)	49
45.2.1.8.2	PMD transmit disable 4, 5, 6, 7, 8 through 13 (1.9.5, 1.9.6, 1.9.7, 1.9.8, 1.9.9 through 1.9.14)	50
45.2.1.9	PMD receive signal detect register (Register 1.10)	50
45.2.1.9.1	PMD receive signal detect 914 (1.10.1015)	50
45.2.1.9.2	PMD receive signal detect 4, 5, 6, 7, 8 through 13 (1.10.5, 1.10.6, 1.10.7, 1.10.8, 1.10.9 through 1.10.14)	51
45.2.1.10	PMA/PMD extended ability register (Register 1.11)	51
45.2.1.10.aab	200G/400G extended abilities (1.11.13)	51
45.2.1.14e	200G PMA/PMD extended ability register (Register 1.23)	51
45.2.1.14e.1	200G PMA remote loopback ability (1.23.15)	52
45.2.1.14e.2	200GBASE-LR4 ability (1.23.5)	52
45.2.1.14e.3	200GBASE-FR4 ability (1.23.4)	52
45.2.1.14e.4	200GBASE-DR4 ability (1.23.3)	52
45.2.1.14f	400G PMA/PMD extended ability register (Register 1.24)	52
45.2.1.14f.1	400G PMA remote loopback ability (1.24.15)	53
45.2.1.14f.2	400GBASE-LR8 ability (1.24.5)	53
45.2.1.14f.3	400GBASE-FR8 ability (1.24.4)	53
45.2.1.14f.4	400GBASE-DR4 ability (1.24.3)	53
45.2.1.14f.5	400GBASE-SR16 ability (1.24.2)	53
45.2.1.14g	PMD transmit disable extension register (Register 1.27)	53
45.2.1.14g.1	PMD transmit disable 15 (1.27.0)	54
45.2.1.14h	PMD receive signal detect extension register (Register 1.28)	54
45.2.1.14h.1	PMD receive signal detect 15 (1.28.0)	54
45.2.1.116a	200GAUI-8 and 400GAUI-16 chip-to-module recommended CTLE, lane 0 register (Register 1.400)	55
45.2.1.116a.1	Recommended CTLE peaking (1.400.4:1)	55
45.2.1.116b	200GAUI-8 and 400GAUI-16 chip-to-module recommended CTLE, lane 1 through lane 7 registers (Registers 1.401 through 1.407)	55
45.2.1.116c	400GAUI-16 chip-to-module recommended CTLE, lane 8 through lane 15 registers (Registers 1.408 through 1.415)	55
45.2.1.116d	200GAUI-n and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 register (Register 1.500)	56
45.2.1.116d.1	Request flag (1.500.15)	57
45.2.1.116d.2	Post-cursor request (1.500.14:12)	57
45.2.1.116d.3	Pre-cursor request (1.500.11:10)	57
45.2.1.116d.4	Post-cursor remote setting (1.500.9:7)	57
45.2.1.116d.5	Pre-cursor remote setting (1.500.6:5)	57
45.2.1.116d.6	Post-cursor local setting (1.500.4:2)	57
45.2.1.116d.7	Pre-cursor local setting (1.500.1:0)	57
45.2.1.116e	200GAUI-n and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 1 through lane 15 registers (Registers 1.501 through 1.515)	58
45.2.1.116f	200GAUI-n and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 0 register (Register 1.516)	58
45.2.1.116f.1	Request flag (1.516.15)	59
45.2.1.116f.2	Post-cursor request (1.516.14:12)	59
45.2.1.116f.3	Pre-cursor request (1.516.11:10)	59
45.2.1.116f.4	Post-cursor remote setting (1.516.9:7)	59
45.2.1.116f.5	Pre-cursor remote setting (1.516.6:5)	60
45.2.1.116f.6	Post-cursor local setting (1.516.4:2)	60
45.2.1.116f.7	Pre-cursor local setting (1.516.1:0)	60

45.2.1.116g	200GAUI-n and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 1 through lane 15 registers (Registers 1.517 through 1.531)	60
45.2.1.123	Test-pattern ability (Register 1.1500)	60
45.2.1.124	PRBS pattern testing control (Register 1.1501)	62
45.2.1.125	Square wave testing control (Register 1.1510)	63
45.2.1.125a	PRBS13Q testing control (Register 1.1512)	64
45.2.1.126	PRBS Tx pattern testing error counter (Register 1.1600 through 1,1615, 1.1601, 1.1602, 1.1603, 1.1604, 1.1605, 1.1606, 1.1607, 1.1608, 1.1609)	65
45.2.1.127	PRBS Rx pattern testing error counter (Register 1.1700 through 1.1715, 1.1701, 1.1702, 1.1703, 1.1704, 1.1705, 1.1706, 1.1707, 1.1708, 1.1709)	66
45.2.3	PCS registers	66
45.2.3.1	PCS control 1 register (Register 3.0)	67
45.2.3.2	PCS status 1 register (Register 3.1)	67
45.2.3.2.7	PCS receive link status (3.1.2)	67
45.2.3.4	PCS speed ability (Register 3.4)	67
45.2.3.4.8	200G capable (3.4.8)	68
45.2.3.4.9	400G capable (3.4.9)	68
45.2.3.6	PCS control 2 register (Register 3.7)	68
45.2.3.6.1	PCS type selection (3.7.3:0)	69
45.2.3.7a	PCS status 3 register (Register 3.9)	69
45.2.3.7a.1	400GBASE-R capable (3.9.1)	69
45.2.3.7a.2	200GBASE-R capable (3.9.0)	69
45.2.3.9a	EEE control and capability 2 (Register 3.21)	69
45.2.3.9a.a	400GBASE-R EEE fast wake supported (3.21.5)	70
45.2.3.9a.b	200GBASE-R EEE fast wake supported (3.21.3)	70
45.2.3.13	BASE-R and MultiGBASE-T PCS status 1 register (Register 3.32)	70
45.2.3.13.1	BASE-R and MultiGBASE-T receive link status (3.32.12)	70
45.2.3.17	BASE-R PCS test-pattern control register (Register 3.42)	70
45.2.3.46	Lane 0 mapping register (Register 3.400)	70
45.2.3.47h	PCS FEC symbol error counter lane 0 (Register 3.600, 3.601)	71
45.2.3.47i	PCS FEC symbol error counter lane 1 through 15 (Registers 3.602 through 3.631)	71
45.2.3.47j	PCS FEC control register (Register 3.800)	71
45.2.3.47j.1	PCS FEC degraded SER enable (3.800.2)	72
45.2.3.47j.2	PCS FEC bypass indication enable (3.800.1)	72
45.2.3.47k	PCS FEC status register (Register 3.801)	72
45.2.3.47k.1	Local degraded SER received (3.801.6)	72
45.2.3.47k.2	Remote degraded SER received (3.801.5)	73
45.2.3.47k.3	PCS FEC degraded SER (3.801.4)	73
45.2.3.47k.4	PCS FEC degraded SER ability (3.801.3)	73
45.2.3.47k.5	PCS FEC high SER (3.801.2)	73
45.2.3.47k.6	PCS FEC bypass indication ability (3.801.1)	73
45.2.3.47l	PCS FEC corrected codewords counter (Register 3.802, 3.803)	73
45.2.3.47m	PCS FEC uncorrected codewords counter (Register 3.804, 3.805)	74
45.2.3.47n	PCS FEC degraded SER activate threshold register (Register 3.806, 3.807)	74
45.2.3.47o	PCS FEC degraded SER deactivate threshold register (Register 3.808, 3.809)	74
45.2.3.47p	PCS FEC degraded SER interval register (Register 3.810, 3.811)	75
45.2.4	PHY XS registers	75
45.2.4.1	PHY XS control 1 register (Register 4.0)	76
45.2.4.4	PHY XS speed ability (Register 4.4)	76
45.2.4.4.a	400G capable (4.4.9)	77
45.2.4.4.b	200G capable (4.4.8)	77
45.2.4.11a	BASE-R PHY XS status 1 register (Register 4.32)	77
45.2.4.11a.1	BASE-R PHY XS receive link status (4.32.12)	77

45.2.4.11b	BASE-R PHY XS test-pattern control register (Register 4.42)	78
45.2.4.11b.1	Transmit test-pattern enable (4.42.3)	78
45.2.4.11c	Multi-lane BASE-R PHY XS alignment status 1 register (Register 4.50)	78
45.2.4.11c.1	PHY XS lane alignment status (4.50.12)	78
45.2.4.11d	Multi-lane BASE-R PHY XS alignment status 3 register (Register 4.52)	79
45.2.4.11d.1	Lane 7 aligned (4.52.7)	79
45.2.4.11d.2	Lane 6 aligned (4.52.6)	79
45.2.4.11d.3	Lane 5 aligned (4.52.5)	79
45.2.4.11d.4	Lane 4 aligned (4.52.4)	80
45.2.4.11d.5	Lane 3 aligned (4.52.3)	80
45.2.4.11d.6	Lane 2 aligned (4.52.2)	80
45.2.4.11d.7	Lane 1 aligned (4.52.1)	80
45.2.4.11d.8	Lane 0 aligned (4.52.0)	80
45.2.4.11e	Multi-lane BASE-R PHY XS alignment status 4 register (Register 4.53)	80
45.2.4.11e.1	Lane 15 aligned (4.53.7)	81
45.2.4.11e.2	Lane 14 aligned (4.53.6)	81
45.2.4.11e.3	Lane 13 aligned (4.53.5)	81
45.2.4.11e.4	Lane 12 aligned (4.53.4)	81
45.2.4.11e.5	Lane 11 aligned (4.53.3)	81
45.2.4.11e.6	Lane 10 aligned (4.53.2)	82
45.2.4.11e.7	Lane 9 aligned (4.53.1)	82
45.2.4.11e.8	Lane 8 aligned (4.53.0)	82
45.2.4.11f	PHY XS lane mapping, lane 0 register (Register 4.400)	82
45.2.4.11g	PHY XS lane mapping, lane 1 through lane 15 registers (Registers 4.401 through 4.415)	82
45.2.4.11h	PHY XS FEC symbol error counter lane 0 (Register 4.600, 4.601)	82
45.2.4.11i	PHY XS FEC symbol error counter lane 1 through 15 (Registers 4.602 through 4.631)	83
45.2.4.11j	PHY XS FEC control register (Register 4.800)	83
45.2.4.11j.1	PHY XS FEC degraded SER enable (4.800.2)	83
45.2.4.11j.2	PHY XS FEC bypass indication enable (4.800.1)	83
45.2.4.11k	PHY XS FEC status register (Register 4.801)	84
45.2.4.11k.1	Remote degraded SER received (4.801.5)	84
45.2.4.11k.2	PHY XS FEC degraded SER (4.801.4)	84
45.2.4.11k.3	PHY XS FEC degraded SER ability (4.801.3)	84
45.2.4.11k.4	PHY XS FEC high SER (4.801.2)	85
45.2.4.11k.5	PHY XS FEC bypass indication ability (4.801.1)	85
45.2.4.11l	PHY XS FEC corrected codewords counter (Register 4.802, 4.803)	85
45.2.4.11m	PHY XS FEC uncorrected codewords counter (Register 4.804, 4.805)	85
45.2.4.11n	PHY XS FEC degraded SER activate threshold register (Register 4.806, 4.807)	86
45.2.4.11o	PHY XS FEC degraded SER deactivate threshold register (Register 4.808, 4.809)	86
45.2.4.11p	PHY XS FEC degraded SER interval register (Register 4.810, 4.811)	86
45.2.5	DTE XS registers	87
45.2.5.1	DTE XS control 1 register (Register 5.0)	88
45.2.5.4	DTE XS speed ability (Register 5.4)	88
45.2.5.4.a	400G capable (5.4.9)	88
45.2.5.4.b	200G capable (5.4.8)	89
45.2.5.11a	BASE-R DTE XS status 1 register (Register 5.32)	89
45.2.5.11a.1	BASE-R DTE XS receive link status (5.32.12)	89
45.2.5.11b	BASE-R DTE XS test-pattern control register (Register 5.42)	89
45.2.5.11b.1	Transmit test-pattern enable (5.42.3)	90
45.2.5.11c	Multi-lane BASE-R DTE XS alignment status 1 register (Register 5.50)	90

45.2.5.11c.1	DTE XS lane alignment status (5.50.12)	90
45.2.5.11d	Multi-lane BASE-R DTE XS alignment status 3 register (Register 5.52)	90
45.2.5.11d.1	Lane 7 aligned (5.52.7)	91
45.2.5.11d.2	Lane 6 aligned (5.52.6)	91
45.2.5.11d.3	Lane 5 aligned (5.52.5)	91
45.2.5.11d.4	Lane 4 aligned (5.52.4)	91
45.2.5.11d.5	Lane 3 aligned (5.52.3)	91
45.2.5.11d.6	Lane 2 aligned (5.52.2)	92
45.2.5.11d.7	Lane 1 aligned (5.52.1)	92
45.2.5.11d.8	Lane 0 aligned (5.52.0)	92
45.2.5.11e	Multi-lane BASE-R DTE XS alignment status 4 register (Register 5.53)	92
45.2.5.11e.1	Lane 15 aligned (5.53.7)	93
45.2.5.11e.2	Lane 14 aligned (5.53.6)	93
45.2.5.11e.3	Lane 13 aligned (5.53.5)	93
45.2.5.11e.4	Lane 12 aligned (5.53.4)	93
45.2.5.11e.5	Lane 11 aligned (5.53.3)	93
45.2.5.11e.6	Lane 10 aligned (5.53.2)	93
45.2.5.11e.7	Lane 9 aligned (5.53.1)	93
45.2.5.11e.8	Lane 8 aligned (5.53.0)	93
45.2.5.11f	DTE XS lane mapping, lane 0 register (Register 5.400)	93
45.2.5.11g	DTE XS lane mapping, lane 1 through lane 15 registers (Registers 5.401 through 5.415)	94
45.2.5.11h	DTE XS FEC symbol error counter lane 0 (Register 5.600, 5.601)	94
45.2.5.11i	DTE XS FEC symbol error counter lane 1 through 15 (Registers 5.602 through 5.631)	94
45.2.5.11j	DTE XS FEC control register (Register 5.800)	95
45.2.5.11j.1	DTE XS FEC degraded SER enable (5.800.2)	95
45.2.5.11j.2	DTE XS FEC bypass indication enable (5.800.1)	95
45.2.5.11k	DTE XS FEC status register (Register 5.801)	95
45.2.5.11k.1	Local degraded SER received (5.801.6)	96
45.2.5.11k.2	Remote degraded SER received (5.801.5)	96
45.2.5.11k.3	DTE XS FEC degraded SER (5.801.4)	96
45.2.5.11k.4	DTE XS FEC degraded SER ability (5.801.3)	96
45.2.5.11k.5	DTE XS FEC high SER (5.801.2)	96
45.2.5.11k.6	DTE XS FEC bypass indication ability (5.801.1)	97
45.2.5.11l	DTE XS FEC corrected codewords counter (Register 5.802, 5.803)	97
45.2.5.11m	DTE XS FEC uncorrected codewords counter (Register 5.804, 5.805)	97
45.2.5.11n	DTE XS FEC degraded SER activate threshold register (Register 5.806, 5.807)	97
45.2.5.11o	DTE XS FEC degraded SER deactivate threshold register (Register 5.808, 5.809)	98
45.2.5.11p	DTE XS FEC degraded SER interval register (Register 5.810, 5.811)	98
78.	Energy-Efficient Ethernet (EEE)	99
78.1	Overview	99
78.1.4	PHY types optionally supporting EEE	99
78.5	Communication link access latency	100
78.5.1	10 Gb/s PHY extension using extender sublayers XGXS	100
90.	Ethernet support for time synchronization protocols	101
90.1	Introduction	101

116. Introduction to 200 Gb/s and 400 Gb/s networks	102
116.1 Overview	102
116.1.1 Scope	102
116.1.2 Relationship of 200 Gigabit and 400 Gigabit Ethernet to the ISO OSI reference model	102
116.1.3 Nomenclature	103
116.1.4 Physical Layer signaling systems	104
116.2 Summary of 200 Gigabit and 400 Gigabit Ethernet sublayers	105
116.2.1 Reconciliation Sublayer (RS) and Media Independent Interface	105
116.2.2 200GMII and 400GMII Extender Sublayers (200GXS and 400GXS)	105
116.2.3 Physical Coding Sublayer (PCS)	106
116.2.4 Physical Medium Attachment (PMA) sublayer	106
116.2.5 Physical Medium Dependent (PMD) sublayer	106
116.2.6 Management interface (MDIO/MDC)	106
116.2.7 Management	106
116.3 Service interface specification method and notation	106
116.3.1 Inter-sublayer service interface	107
116.3.2 Instances of the Inter-sublayer service interface	107
116.3.3 Semantics of inter-sublayer service interface primitives	107
116.3.3.1 IS_UNITDATA_i.request	107
116.3.3.1.1 Semantics of the service primitive	108
116.3.3.1.2 When generated	109
116.3.3.1.3 Effect of receipt	109
116.3.3.2 IS_UNITDATA_i.indication	110
116.3.3.2.1 Semantics of the service primitive	110
116.3.3.2.2 When generated	110
116.3.3.2.3 Effect of receipt	110
116.3.3.3 IS_SIGNAL.indication	110
116.3.3.3.1 Semantics of the service primitive	110
116.3.3.3.2 When generated	110
116.3.3.3.3 Effect of receipt	110
116.4 Delay constraints	111
116.5 Skew constraints	112
116.6 FEC Degrade	115
116.7 State diagrams	116
116.8 Protocol implementation conformance statement (PICS) proforma	117
117. Reconciliation Sublayer (RS) and Media Independent Interface for 200 Gb/s and 400 Gb/s operation (200GMII and 400GMII)	118
117.1 Overview	118
117.1.1 Summary of major concepts	119
117.1.2 Application	119
117.1.3 Rate of operation	119
117.1.4 Delay constraints	119
117.1.5 Allocation of functions	120
117.1.6 200GMII/400GMII structure	120
117.1.7 Mapping of 200GMII/400GMII signals to PLS service primitives	120
117.2 200GMII/400GMII data stream	120
117.3 200GMII/400GMII functional specifications	120
117.4 LPI Assertion and Detection	120

117.5	Protocol implementation conformance statement (PICS) proforma for Clause 117, Reconciliation Sublayer (RS) and Media Independent Interface for 200 Gb/s and 400 Gb/s operation (200GMII and 400GMII).....	121
117.5.1	Introduction.....	121
117.5.2	Identification.....	121
117.5.2.1	Implementation identification.....	121
117.5.2.2	Protocol summary.....	121
117.5.3	Major capabilities/options.....	122
117.5.4	PICS proforma tables for Reconciliation Sublayer (RS) and Media Independent Interface for 200 Gb/s and 400 Gb/s operation (200GMII and 400GMII).....	122
117.5.4.1	General.....	122
117.5.4.2	Mapping of PLS service primitives.....	122
117.5.4.3	Data stream structure.....	123
117.5.4.4	200GMII/400GMII signal functional specifications.....	123
117.5.4.5	Link fault signaling state diagram.....	124
117.5.4.6	LPI functions.....	124
118.	200GMII Extender, 400GMII Extender, 200GMII Extender Sublayer (200GXS), and 400GMII Extender Sublayer (400GXS).....	125
118.1	Overview.....	125
118.1.1	Summary of major concepts.....	126
118.1.2	200GXS/400GXS Sublayer.....	126
118.1.3	200GAUI-n/400GAUI-n.....	126
118.2	FEC Degrade.....	126
118.2.1	DTE XS FEC Degrade signaling.....	126
118.2.2	PHY XS FEC Degrade signaling.....	127
118.3	200GXS and 400GXS partitioning example.....	127
118.4	200GXS and 400GXS MDIO function mapping.....	127
118.5	Protocol implementation conformance statement (PICS) proforma for Clause 118, 200GMII Extender, 400GMII Extender, 200GMII Extender Sublayer (200GXS), and 400GMII Extender Sublayer (400GXS).....	131
118.5.1	Introduction.....	131
118.5.2	Identification.....	131
118.5.2.1	Implementation identification.....	131
118.5.2.2	Protocol summary.....	131
118.5.3	Major capabilities/options.....	132
118.5.4	PICS proforma tables for 200GMII Extender, 400GMII Extender, 200GMII Extender Sublayer (200GXS), and 400GMII Extender Sublayer (400GXS).....	132
118.5.4.1	Transmit function.....	132
118.5.4.2	Receive function.....	133
118.5.4.3	64B/66B coding rules.....	133
118.5.4.4	Scrambler and descrambler.....	134
118.5.4.5	Alignment markers.....	134
118.5.5	Test-pattern modes.....	134
118.5.6	Bit order.....	134
118.5.7	Management.....	135
118.5.7.1	State diagrams.....	135
118.5.7.2	Loopback.....	135
118.5.7.3	Delay constraints.....	136
119.	Physical Coding Sublayer (PCS) for 64B/66B, type 200GBASE-R and 400GBASE-R.....	137
119.1	Overview.....	137

119.1.1	Scope.....	137
119.1.2	Relationship of 200GBASE-R and 400GBASE-R to other standards	137
119.1.3	Physical Coding Sublayer (PCS)	137
119.1.4	Inter-sublayer interfaces	138
119.1.4.1	PCS service interface (200GMII/400GMII).....	138
119.1.4.2	Physical Medium Attachment (PMA) service interface	138
119.1.5	Functional block diagram	139
119.2	Physical Coding Sublayer (PCS)	140
119.2.1	Functions within the PCS	140
119.2.2	Use of blocks	140
119.2.3	64B/66B code	141
119.2.3.1	Notation conventions	141
119.2.3.2	64B/66B block structure	141
119.2.3.3	Control codes	141
119.2.3.4	Valid and invalid blocks	142
119.2.3.5	Idle (/I/).....	142
119.2.3.6	Start (/S/).....	142
119.2.3.7	Terminate (/T/).....	142
119.2.3.8	Ordered set (/O/).....	142
119.2.3.9	Error (/E/).....	142
119.2.4	Transmit.....	142
119.2.4.1	Encode and rate matching.....	142
119.2.4.2	64B/66B to 256B/257B transcoder.....	143
119.2.4.3	Scrambler	145
119.2.4.4	Alignment marker mapping and insertion	145
119.2.4.4.1	AM creation for the 200GBASE-R PCS	146
119.2.4.4.2	AM creation for the 400GBASE-R PCS	148
119.2.4.5	Pre-FEC distribution	150
119.2.4.6	Reed-Solomon encoder.....	150
119.2.4.7	Symbol distribution.....	152
119.2.4.8	Transmit bit ordering and distribution	153
119.2.4.9	Test-pattern generators	155
119.2.5	Receive function	155
119.2.5.1	Alignment lock and deskew.....	155
119.2.5.2	Lane reorder and de-interleave	155
119.2.5.3	Reed-Solomon decoder.....	155
119.2.5.4	Post FEC interleave	156
119.2.5.5	Alignment marker removal.....	156
119.2.5.6	Descrambler.....	156
119.2.5.7	256B/257B to 64B/66B transcoder.....	157
119.2.5.8	Decode and rate matching.....	157
119.2.6	Detailed functions and state diagrams	158
119.2.6.1	State diagram conventions.....	158
119.2.6.2	State variables	158
119.2.6.2.1	Constants.....	158
119.2.6.2.2	Variables	158
119.2.6.2.3	Functions.....	160
119.2.6.2.4	Counters	162
119.2.6.3	State diagrams.....	162
119.3	PCS management.....	167
119.3.1	PCS MDIO function mapping	167
119.4	Loopback	168
119.5	Delay constraints.....	168

119.6	Protocol implementation conformance statement (PICS) proforma for Clause 119, Physical Coding Sublayer (PCS) for 64B/66B, type 200GBASE-R and 400GBASE-R.....	169
119.6.1	Introduction.....	169
119.6.2	Identification.....	169
119.6.2.1	Implementation identification.....	169
119.6.2.2	Protocol summary.....	169
119.6.3	Major capabilities/options.....	170
119.6.4	PICS proforma tables for Physical Coding Sublayer (PCS) 64B/66B, type 200GBASE-R and 400GBASE-R.....	170
119.6.4.1	Transmit function.....	170
119.6.4.2	Receive function.....	171
119.6.4.3	64B/66B coding rules.....	171
119.6.4.4	Scrambler and descrambler.....	172
119.6.4.5	Alignment markers.....	172
119.6.4.6	Test-pattern modes.....	172
119.6.4.7	Bit order.....	173
119.6.4.8	Management.....	173
119.6.4.9	State diagrams.....	173
119.6.4.10	Loopback.....	173
119.6.4.11	Delay constraints.....	174
120.	Physical Medium Attachment (PMA) sublayer, type 200GBASE-R and 400GBASE-R.....	175
120.1	Overview.....	175
120.1.1	Scope.....	175
120.1.2	Position of the PMA in the 200GBASE-R and 400GBASE-R sublayers.....	175
120.1.3	Summary of functions.....	175
120.1.4	PMA sublayer positioning.....	176
120.2	PMA interfaces.....	178
120.3	PMA service interface.....	178
120.4	Service interface below PMA.....	181
120.5	Functions within the PMA.....	182
120.5.1	Per input-lane clock and data recovery.....	182
120.5.2	Bit-level multiplexing.....	182
120.5.3	Skew and Skew Variation.....	183
120.5.3.1	Skew generation toward SP1.....	183
120.5.3.2	Skew tolerance at SP1.....	183
120.5.3.3	Skew generation toward SP2.....	183
120.5.3.4	Skew tolerance at SP5.....	185
120.5.3.5	Skew generation at SP6.....	185
120.5.3.6	Skew tolerance at SP6.....	185
120.5.4	Delay constraints.....	185
120.5.5	Clocking architecture.....	185
120.5.6	Signal drivers.....	186
120.5.7	Gray mapping for PAM4 encoded lanes.....	186
120.5.8	Link status.....	186
120.5.9	PMA local loopback mode (optional).....	187
120.5.10	PMA remote loopback mode (optional).....	187
120.5.11	PMA test patterns (optional).....	187
120.5.11.1	Test patterns for NRZ encoded signals.....	188
120.5.11.1.1	PRBS31 test pattern.....	188
120.5.11.1.2	PRBS9 test pattern.....	189
120.5.11.1.3	Square wave test pattern.....	189
120.5.11.2	Test patterns for PAM4 encoded signals.....	189

120.5.11.2.1	PRBS13Q test pattern	190
120.5.11.2.2	PRBS31Q test pattern	190
120.5.11.2.3	SSPRQ test pattern.....	192
120.5.11.2.4	Square wave (quaternary) test pattern	193
120.6	PMA MDIO function mapping.....	193
120.7	Protocol implementation conformance statement (PICS) proforma for Clause 120, Physical Medium Attachment (PMA) sublayer, type 200GBASE-R and 400GBASE-R	198
120.7.1	Introduction.....	198
120.7.2	Identification.....	198
120.7.2.1	Implementation identification.....	198
120.7.2.2	Protocol summary.....	198
120.7.3	Major capabilities/options.....	199
120.7.4	Skew generation and tolerance	201
120.7.5	Test patterns.....	201
120.7.6	Loopback modes.....	202
121.	Physical Medium Dependent (PMD) sublayer and medium, type 200GBASE-DR4	203
121.1	Overview.....	203
121.1.1	Bit error ratio	203
121.2	Physical Medium Dependent (PMD) service interface	204
121.3	Delay and Skew	205
121.3.1	Delay constraints.....	205
121.3.2	Skew constraints	205
121.4	PMD MDIO function mapping.....	206
121.5	PMD functional specifications.....	206
121.5.1	PMD block diagram.....	206
121.5.2	PMD transmit function	207
121.5.3	PMD receive function.....	207
121.5.4	PMD global signal detect function	207
121.5.5	PMD lane-by-lane signal detect function	208
121.5.6	PMD reset function.....	208
121.5.7	PMD global transmit disable function (optional)	208
121.5.8	PMD lane-by-lane transmit disable function (optional)	209
121.5.9	PMD fault function (optional)	209
121.5.10	PMD transmit fault function (optional)	209
121.5.11	PMD receive fault function (optional).....	209
121.6	Lane assignments.....	209
121.7	PMD to MDI optical specifications for 200GBASE-DR4	209
121.7.1	200GBASE-DR4 transmitter optical specifications	210
121.7.2	200GBASE-DR4 receive optical specifications	210
121.7.3	200GBASE-DR4 illustrative link power budget	211
121.8	Definition of optical parameters and measurement methods.....	212
121.8.1	Test patterns for optical parameters.....	212
121.8.2	Wavelength	212
121.8.3	Average optical power	213
121.8.4	Outer Optical Modulation Amplitude (OMA _{outer}).....	213
121.8.5	Transmitter and dispersion eye closure for PAM4 (TDECQ).....	213
121.8.5.1	TDECQ conformance test setup	213
121.8.5.2	Channel requirements	214
121.8.5.3	TDECQ measurement method.....	215
121.8.5.4	TDECQ reference equalizer.....	218
121.8.6	Extinction ratio	218
121.8.7	Relative intensity noise (RIN _{21.4OMA}).....	218

121.8.8	Receiver sensitivity	218
121.8.9	Stressed receiver sensitivity	218
121.8.9.1	Stressed receiver conformance test block diagram	219
121.8.9.2	Stressed receiver conformance test signal characteristics and calibration	220
121.8.9.3	Stressed receiver conformance test signal verification	220
121.8.9.4	Sinusoidal jitter for receiver conformance test	221
121.9	Safety, installation, environment, and labeling	221
121.9.1	General safety	221
121.9.2	Laser safety	222
121.9.3	Installation	222
121.9.4	Environment	222
121.9.5	Electromagnetic emission	222
121.9.6	Temperature, humidity, and handling	222
121.9.7	PMD labeling requirements	222
121.10	Fiber optic cabling model	223
121.11	Characteristics of the fiber optic cabling (channel)	223
121.11.1	Optical fiber cable	224
121.11.2	Optical fiber connection	224
121.11.2.1	Connection insertion loss	224
121.11.2.2	Maximum discrete reflectance	224
121.11.3	Medium Dependent Interface (MDI)	225
121.11.3.1	Optical lane assignments	225
121.11.3.2	Medium Dependent Interface (MDI) requirements	225
121.12	Protocol implementation conformance statement (PICS) proforma for Clause 121, Physical Medium Dependent (PMD) sublayer and medium, type 200GBASE-DR4	226
121.12.1	Introduction	226
121.12.2	Identification	226
121.12.2.1	Implementation identification	226
121.12.2.2	Protocol summary	226
121.12.3	Major capabilities/options	227
121.12.4	PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 200GBASE-DR4	227
121.12.4.1	PMD functional specifications	227
121.12.4.2	Management functions	228
121.12.4.3	PMD to MDI optical specifications for 200GBASE-DR4	228
121.12.4.4	Optical measurement methods	229
121.12.4.5	Environmental specifications	229
121.12.4.6	Characteristics of the fiber optic cabling and MDI	229
122.	Physical Medium Dependent (PMD) sublayer and medium, type 200GBASE-FR4, 200GBASE- LR4, 400GBASE-FR8, and 400GBASE-LR8	230
122.1	Overview	230
122.1.1	Bit error ratio	231
122.2	Physical Medium Dependent (PMD) service interface	232
122.3	Delay and Skew	232
122.3.1	Delay constraints	232
122.3.2	Skew constraints	232
122.4	PMD MDIO function mapping	233
122.5	PMD functional specifications	234
122.5.1	PMD block diagram	234
122.5.2	PMD transmit function	234
122.5.3	PMD receive function	235
122.5.4	PMD global signal detect function	235

122.5.5	PMD lane-by-lane signal detect function	236
122.5.6	PMD reset function	236
122.5.7	PMD global transmit disable function (optional)	236
122.5.8	PMD lane-by-lane transmit disable function	236
122.5.9	PMD fault function (optional)	236
122.5.10	PMD transmit fault function (optional)	236
122.5.11	PMD receive fault function (optional)	237
122.6	Wavelength-division-multiplexed lane assignments	237
122.7	PMD to MDI optical specifications for 200GBASE-FR4, 200GBASE-LR4, 400GBASE-FR8, and 400GBASE-LR8	238
122.7.1	200GBASE-FR4, 200GBASE-LR4, 400GBASE-FR8, and 400GBASE-LR8 transmitter optical specifications	238
122.7.2	200GBASE-FR4, 200GBASE-LR4, 400GBASE-FR8, and 400GBASE-LR8 receive optical specifications	241
122.7.3	200GBASE-FR4, 200GBASE-LR4, 400GBASE-FR8, and 400GBASE-LR8 illustrative link power budgets	243
122.8	Definition of optical parameters and measurement methods	243
122.8.1	Test patterns for optical parameters	243
122.8.2	Wavelength	244
122.8.3	Average optical power	244
122.8.4	Outer Optical Modulation Amplitude (OMA _{outer})	244
122.8.5	Transmitter and dispersion eye closure for PAM4 (TDECQ)	245
122.8.5.1	TDECQ conformance test setup	245
122.8.5.2	Channel requirements	246
122.8.5.3	TDECQ measurement method	247
122.8.5.4	TDECQ reference equalizer	247
122.8.6	Extinction ratio	247
122.8.7	Relative intensity noise (RIN _{16.5OMA} and RIN _{15.1OMA})	247
122.8.8	Receiver sensitivity	247
122.8.9	Stressed receiver sensitivity	247
122.8.9.1	Stressed receiver conformance test block diagram	248
122.8.9.2	Stressed receiver conformance test signal characteristics and calibration	248
122.8.9.3	Stressed receiver conformance test signal verification	248
122.9	Safety, installation, environment, and labeling	249
122.9.1	General safety	249
122.9.2	Laser safety	249
122.9.3	Installation	250
122.9.4	Environment	250
122.9.5	Electromagnetic emission	250
122.9.6	Temperature, humidity, and handling	250
122.9.7	PMD labeling requirements	250
122.10	Fiber optic cabling model	251
122.11	Characteristics of the fiber optic cabling (channel)	252
122.11.1	Optical fiber cable	252
122.11.2	Optical fiber connection	252
122.11.2.1	Connection insertion loss	252
122.11.2.2	Maximum discrete reflectance	252
122.11.3	Medium Dependent Interface (MDI) requirements	253
122.12	Protocol implementation conformance statement (PICS) proforma for Clause 122, Physical Medium Dependent (PMD) sublayer and medium, type 200GBASE-FR4, 200GBASE- LR4, 400GBASE-FR8, and 400GBASE-LR8	254
122.12.1	Introduction	254
122.12.2	Identification	254
122.12.2.1	Implementation identification	254

122.12.2.2	Protocol summary	254
122.12.3	Major capabilities/options.....	255
122.12.4	PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 200GBASE-FR4, 200GBASE-LR4, 400GBASE-FR8, and 400GBASE-LR8	255
122.12.4.1	PMD functional specifications.....	255
122.12.4.2	Management functions.....	256
122.12.4.3	PMD to MDI optical specifications for 200GBASE-FR4	257
122.12.4.4	PMD to MDI optical specifications for 200GBASE-LR4	257
122.12.4.5	PMD to MDI optical specifications for 400GBASE-FR8	257
122.12.4.6	PMD to MDI optical specifications for 400GBASE-LR8.....	257
122.12.4.7	Optical measurement methods.....	258
122.12.4.8	Environmental specifications.....	258
122.12.4.9	Characteristics of the fiber optic cabling and MDI.....	258
123.	Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-SR16	259
123.1	Overview.....	259
123.1.1	Bit error ratio	260
123.2	Physical Medium Dependent (PMD) service interface	260
123.3	Delay and Skew	261
123.3.1	Delay constraints.....	261
123.3.2	Skew constraints	261
123.4	PMD MDIO function mapping.....	262
123.5	PMD functional specifications.....	262
123.5.1	PMD block diagram	262
123.5.2	PMD transmit function	263
123.5.3	PMD receive function.....	263
123.5.4	PMD global signal detect function	264
123.5.5	PMD lane-by-lane signal detect function	264
123.5.6	PMD reset function.....	264
123.5.7	PMD global transmit disable function (optional)	265
123.5.8	PMD lane-by-lane transmit disable function (optional)	265
123.5.9	PMD fault function (optional)	265
123.5.10	PMD transmit fault function (optional)	265
123.5.11	PMD receive fault function (optional).....	265
123.6	Lane assignments.....	265
123.7	PMD to MDI optical specifications for 400GBASE-SR16	266
123.7.1	400GBASE-SR16 transmitter optical specifications	266
123.7.2	400GBASE-SR16 receive optical specifications.....	266
123.7.3	400GBASE-SR16 illustrative link power budget.....	266
123.8	Definition of optical parameters and measurement methods.....	266
123.8.1	Test patterns for optical parameters.....	266
123.8.2	Center wavelength and spectral width.....	267
123.8.3	Average optical power	267
123.8.4	Optical Modulation Amplitude (OMA).....	267
123.8.5	Transmitter and dispersion eye closure (TDEC)	267
123.8.6	Extinction ratio	267
123.8.7	Transmitter optical waveform (transmit eye)	267
123.8.8	Stressed receiver sensitivity.....	267
123.9	Safety, installation, environment, and labeling.....	268
123.9.1	General safety	268
123.9.2	Laser safety	268
123.9.3	Installation	268

123.9.4	Environment.....	268
123.9.5	Electromagnetic emission	268
123.9.6	Temperature, humidity, and handling.....	268
123.9.7	PMD labeling requirements	269
123.10	Fiber optic cabling model	269
123.11	Characteristics of the fiber optic cabling (channel)	269
123.11.1	Optical fiber cable.....	270
123.11.2	Optical fiber connection.....	270
123.11.2.1	Connection insertion loss.....	270
123.11.2.2	Maximum discrete reflectance.....	270
123.11.3	Medium Dependent Interface (MDI).....	270
123.11.3.1	Optical lane assignments	271
123.11.3.2	Medium Dependent Interface (MDI) requirements	271
123.12	Protocol implementation conformance statement (PICS) proforma for Clause 123, Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-SR16.....	272
123.12.1	Introduction.....	272
123.12.2	Identification.....	272
123.12.2.1	Implementation identification.....	272
123.12.2.2	Protocol summary	272
123.12.3	Major capabilities/options.....	273
123.12.4	PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-SR16.....	273
123.12.4.1	PMD functional specifications.....	273
123.12.4.2	Management functions.....	274
123.12.4.3	PMD to MDI optical specifications for 400GBASE-SR16.....	274
123.12.4.4	Optical measurement methods.....	275
123.12.4.5	Environmental specifications.....	275
123.12.4.6	Characteristics of the fiber optic cabling and MDI.....	275
124.	Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-DR4	277
124.1	Overview.....	277
124.1.1	Bit error ratio	277
124.2	Physical Medium Dependent (PMD) service interface	278
124.3	Delay and Skew	279
124.3.1	Delay constraints.....	279
124.3.2	Skew constraints	279
124.4	PMD MDIO function mapping.....	279
124.5	PMD functional specifications.....	280
124.5.1	PMD block diagram.....	280
124.5.2	PMD transmit function	281
124.5.3	PMD receive function.....	281
124.5.4	PMD global signal detect function	281
124.5.5	PMD lane-by-lane signal detect function	282
124.5.6	PMD reset function.....	282
124.5.7	PMD global transmit disable function (optional)	282
124.5.8	PMD lane-by-lane transmit disable function (optional)	283
124.5.9	PMD fault function (optional)	283
124.5.10	PMD transmit fault function (optional)	283
124.5.11	PMD receive fault function (optional).....	283
124.6	Lane assignments.....	283
124.7	PMD to MDI optical specifications for 400GBASE-DR4	283
124.7.1	400GBASE-DR4 transmitter optical specifications	284
124.7.2	400GBASE-DR4 receive optical specifications	284

124.7.3	400GBASE-DR4 illustrative link power budget	285
124.8	Definition of optical parameters and measurement methods.....	286
124.8.1	Test patterns for optical parameters.....	286
124.8.2	Wavelength	286
124.8.3	Average optical power	287
124.8.4	Outer Optical Modulation Amplitude (OMA _{outer}).....	287
124.8.5	Transmitter and dispersion eye closure for PAM4 (TDECQ).....	287
124.8.6	Extinction ratio	287
124.8.7	Relative intensity noise (RIN _{21.4OMA}).....	288
124.8.8	Receiver sensitivity.....	288
124.8.9	Stressed receiver sensitivity.....	288
124.9	Safety, installation, environment, and labeling.....	288
124.9.1	General safety	288
124.9.2	Laser safety	288
124.9.3	Installation	289
124.9.4	Environment.....	289
124.9.5	Electromagnetic emission	289
124.9.6	Temperature, humidity, and handling.....	289
124.9.7	PMD labeling requirements	289
124.10	Fiber optic cabling model	289
124.11	Characteristics of the fiber optic cabling (channel).....	290
124.11.1	Optical fiber cable.....	290
124.11.2	Optical fiber connection.....	291
124.11.2.1	Connection insertion loss.....	291
124.11.2.2	Maximum discrete reflectance.....	291
124.11.3	Medium Dependent Interface (MDI).....	291
124.11.3.1	Optical lane assignments	291
124.11.3.2	Medium Dependent Interface (MDI) requirements.....	292
124.12	Protocol implementation conformance statement (PICS) proforma for Clause 124, Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-DR4.....	293
124.12.1	Introduction.....	293
124.12.2	Identification.....	293
124.12.2.1	Implementation identification.....	293
124.12.2.2	Protocol summary	293
124.12.3	Major capabilities/options.....	294
124.12.4	PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 400GBASE-DR4	294
124.12.4.1	PMD functional specifications.....	294
124.12.4.2	Management functions.....	295
124.12.4.3	PMD to MDI optical specifications for 400GBASE-DR4	295
124.12.4.4	Optical measurement methods.....	296
124.12.4.5	Environmental specifications.....	296
124.12.4.6	Characteristics of the fiber optic cabling and MDI.....	296
Annex A (informative)	Bibliography	297
Annex 4A (normative)	Simplified full duplex media access control	298
4A.4	Specific implementations.....	298
4A.4.2	MAC parameters.....	298
Annex 31B (normative)	MAC Control PAUSE operation	299
31B.3	Detailed specification of PAUSE operation.....	299

31B.3.7	Timing considerations for PAUSE operation	299
31B.4	Protocol implementation conformance statement (PICS) proforma for MAC Control PAUSE operation	299
31B.4.3	Major capabilities/options.....	299
31B.4.6	PAUSE command MAC timing considerations	300
Annex 93A (normative)	Specification methods for electrical channels	301
93A.1	Channel Operating Margin.....	301
93A.1.2	Transmitter and receiver device package models	302
93A.1.2.3	Two-port network for the package transmission line	302
93A.1.4	Filters	302
93A.1.4.3	Receiver equalizer.....	302
93A.1.6	Determination of variable equalizer parameters	303
93A.1.7	Interference and noise amplitude.....	303
Annex 119A (informative)	200GBASE-R and 400GBASE-R PCS FEC codeword examples	304
Annex 120A (informative)	200 Gb/s and 400 Gb/s PMA sublayer partitioning examples.....	310
120A.1	Partitioning example supporting 400GBASE-SR16	310
120A.2	Partitioning examples supporting 200GBASE-DR4/FR4/LR4 and 400GBASE-FR8/LR8	311
120A.3	Partitioning examples supporting 400GBASE-DR4.....	313
120A.4	Partitioning example using 200GXS and 400GXS.....	314
Annex 120B (normative)	Chip-to-chip 200 Gb/s eight-lane Attachment Unit Interface (200GAUI-8 C2C) and 400 Gb/s sixteen-lane Attachment Unit Interface (400GAUI-16 C2C).....	315
120B.1	Overview	315
120B.2	200GAUI-8 and 400GAUI-16 chip-to-chip compliance point definition	317
120B.3	200GAUI-8 and 400GAUI-16 chip-to-chip electrical characteristics	318
120B.3.1	200GAUI-8 and 400GAUI-16 C2C transmitter characteristics	318
120B.3.2	200GAUI-8 and 400GAUI-16 C2C receiver characteristics	318
120B.4	200GAUI-8 and 400GAUI-16 chip-to-chip channel characteristics	319
120B.5	Protocol implementation conformance statement (PICS) proforma for Annex 120B, Chip- to-chip 200 Gb/s eight-lane Attachment Unit Interface (200GAUI-8 C2C) and 400 Gb/s sixteen-lane Attachment Unit Interface (400GAUI-16 C2C)	320
120B.5.1	Introduction.....	320
120B.5.2	Identification	320
120B.5.2.1	Implementation identification.....	320
120B.5.2.2	Protocol summary	320
120B.5.3	Major capabilities/options.....	321
120B.5.4	PICS proforma tables for Chip-to-chip 200 Gb/s eight-lane Attachment Unit Interface (200GAUI-8 C2C) and 400 Gb/s sixteen-lane Attachment Unit Interface (400GAUI-16 C2C)	321
120B.5.4.1	Transmitter.....	321
120B.5.4.2	Receiver	322
120B.5.4.3	Channel	322
Annex 120C (normative)	Chip-to-module 200 Gb/s eight-lane Attachment Unit Interface (200GAUI-8 C2M) and 400 Gb/s sixteen-lane Attachment Unit Interface (400GAUI-16 C2M).....	323
120C.1	Overview	323

120C.1.1 Bit error ratio	325
120C.2 200GAUI-8 and 400GAUI-16 chip-to-module compliance point definitions	325
120C.3 200GAUI-8 and 400GAUI-16 chip-to-module electrical characteristics	325
120C.3.1 200GAUI-8 and 400GAUI-16 C2M host output characteristics	325
120C.3.2 200GAUI-8 and 400GAUI-16 C2M module output characteristics	325
120C.3.3 200GAUI-8 and 400GAUI-16 C2M host input characteristics	325
120C.3.4 200GAUI-8 and 400GAUI-16 C2M module input characteristics	326
120C.4 200GAUI-8 and 400GAUI-16 C2M measurement methodology	326
120C.5 Protocol implementation conformance statement (PICS) proforma for Annex 120C, Chip-to-module 200 Gb/s eight-lane Attachment Unit Interface (200GAUI-8 C2M) and 400 Gb/s sixteen-lane Attachment Unit Interface (400GAUI-16 C2M)	327
120C.5.1 Introduction	327
120C.5.2 Identification	327
120C.5.2.1 Implementation identification	327
120C.5.2.2 Protocol summary	327
120C.5.3 Major capabilities/options	328
120C.5.4 PICS proforma tables for Chip-to-module 200 Gb/s eight-lane Attachment Unit Interface (200GAUI-8 C2M) and 400 Gb/s sixteen-lane Attachment Unit Interface (400GAUI-16 C2M)	328
120C.5.4.1 Host output	328
120C.5.4.2 Module output	329
120C.5.4.3 Host input	329
120C.5.4.4 Module input	329
 Annex 120D (normative) Chip-to-chip 200 Gb/s four-lane Attachment Unit Interface (200GAUI-4 C2C) and 400 Gb/s eight-lane Attachment Unit Interface (400GAUI-8 C2C)	 330
120D.1 Overview	330
120D.2 200GAUI-4 and 400GAUI-8 chip-to-chip compliance point definition	333
120D.3 200GAUI-4 and 400GAUI-8 chip-to-chip electrical characteristics	333
120D.3.1 200GAUI-4 and 400GAUI-8 C2C transmitter characteristics	333
120D.3.1.1 Transmitter differential output return loss	334
120D.3.1.2 Transmitter linearity	335
120D.3.1.2.1 Measurement of mean signal levels	335
120D.3.1.3 Linear fit to the measured waveform	336
120D.3.1.4 Steady-state voltage and linear fit pulse peak	336
120D.3.1.5 Transmitter equalization settings	336
120D.3.1.6 Transmitter output noise and distortion	338
120D.3.1.7 Transmitter output residual ISI	338
120D.3.1.8 Output jitter	338
120D.3.1.8.1 J _{4u} and J _{RMS} jitter	339
120D.3.1.8.2 Even-odd Jitter	340
120D.3.2 200GAUI-4 and 400GAUI-8 C2C receiver characteristics	340
120D.3.2.1 Receiver interference tolerance	340
120D.3.2.2 Receiver jitter tolerance	342
120D.3.2.3 Transmitter equalization feedback (optional)	342
120D.4 200GAUI-4 and 400GAUI-8 chip-to-chip channel characteristics	343
120D.4.1 Channel Operating Margin	343
120D.4.2 Channel return loss	344
120D.5 Protocol implementation conformance statement (PICS) proforma for Annex 120D, Chip-to-chip 200 Gb/s four-lane Attachment Unit Interface (200GAUI-4 C2C) and 400 Gb/s eight-lane Attachment Unit Interface (400GAUI-8 C2C)	346
120D.5.1 Introduction	346

120D.5.2 Identification	346
120D.5.2.1 Implementation identification	346
120D.5.2.2 Protocol summary	346
120D.5.3 Major capabilities/options.....	347
120D.5.4 PICS proforma tables for Chip-to-chip 200 Gb/s four-lane Attachment Unit Interface (200GAUI-4 C2C) and 400 Gb/s eight-lane Attachment Unit Interface (400GAUI-8 C2C)	347
120D.5.4.1 Transmitter	347
120D.5.4.2 Receiver	348
120D.5.4.3 Channel	348
 Annex 120E (normative) Chip-to-module 200 Gb/s four-lane Attachment Unit Interface (200GAUI-4 C2M) and 400 Gb/s eight-lane Attachment Unit Interface (400GAUI-8 C2M)	 349
120E.1 Overview	349
120E.1.1 Bit error ratio	351
120E.2 200GAUI-4 and 400GAUI-8 chip-to-module compliance point definitions.....	351
120E.3 200GAUI-4 and 400GAUI-8 chip-to-module electrical characteristics	352
120E.3.1 200GAUI-4 and 400GAUI-8 C2M host output characteristics	352
120E.3.1.1 Signaling rate and range	353
120E.3.1.2 Signal levels.....	353
120E.3.1.3 Output return loss.....	354
120E.3.1.4 Differential termination mismatch.....	354
120E.3.1.5 Transition time	354
120E.3.1.6 Host output eye width and eye height.....	354
120E.3.1.7 Reference receiver for eye width and eye height evaluation	355
120E.3.2 200GAUI-4 and 400GAUI-8 C2M module output characteristics.....	357
120E.3.2.1 Module output eye width, eye height, and pre-cursor ISI ratio	358
120E.3.2.1.1 Reference receiver for module output evaluation.....	359
120E.3.2.1.2 Far-end pre-cursor ISI ratio	359
120E.3.3 200GAUI-4 and 400GAUI-8 C2M host input characteristics	359
120E.3.3.1 Input return loss	359
120E.3.3.2 Host stressed input test	360
120E.3.3.2.1 Host stressed input test procedure	360
120E.3.4 200GAUI-4 and 400GAUI-8 C2M module input characteristics.....	362
120E.3.4.1 Module stressed input test.....	362
120E.3.4.1.1 Module stressed input test procedure.....	362
120E.4 200GAUI-4 and 400GAUI-8 C2M measurement methodology.....	364
120E.4.1 HCB/MCB characteristics	364
120E.4.2 Eye width and eye height measurement method	365
120E.5 Protocol implementation conformance statement (PICS) proforma for Annex 120E, Chip- to-module 200 Gb/s four-lane Attachment Unit Interface (200GAUI-4 C2M) and 400 Gb/s eight-lane Attachment Unit Interface (400GAUI-8 C2M)	 368
120E.5.1 Introduction.....	368
120E.5.2 Identification	368
120E.5.2.1 Implementation identification	368
120E.5.2.2 Protocol summary	368
120E.5.3 Major capabilities/options.....	369
120E.5.4 PICS proforma tables for Chip-to-module 200 Gb/s four-lane Attachment Unit Interface (200GAUI-4 C2M) and 400 Gb/s eight-lane Attachment Unit Interface (400GAUI-8 C2M)	 369
120E.5.4.1 Host output.....	369
120E.5.4.2 Module output.....	370

120E.5.4.3 Host input.....	370
120E.5.4.4 Module input.....	370