

IEEE Standard for the Functional Verification Language *e*

IEEE Computer Society

Sponsored by the
Design Automation Standards Committee

IEEE
3 Park Avenue
New York, NY 10016-5997
USA

IEEE Std 1647™-2016
(Revision of
IEEE Std 1647-2011)

IEEE Std 1647™-2016

(Revision of
IEEE Std 1647-2011)

IEEE Standard for the Functional Verification Language *e*

Sponsor

Design Automation Standards Committee
of the
IEEE Computer Society

Approved 30 June 2016

IEEE-SA Standards Board

Grateful acknowledgment is made to Cadence, Inc., for permission to use the following source material:

Namespaces for Types in *e*, Version 1.1

e Language Reference, Version 5.1, Chapter 26 (Encapsulation Constructs)

e Language Reference, Version 9.2, Chapter 6 (Template Types),
Chapter 12 (Generation Constraints), Chapter 21 (Macros)

e Language Reference, Version 10.2, Chapter 2 (*e* Data Types), Chapter 6 (*e* Ports)

e Reuse Methodology Developer Manual, Version 2.1, Chapter 5 (Sequences),
Chapter 6 (Messaging)

e Ports, Chapter 6

Specman Beta Features, Chapter 4 (Constant Fields and Constant when Subtypes),
Chapter 15 (Reflection Interface for *e*)

Abstract: The *e functional verification language* is an application-specific programming language, aimed at automating the task of verifying a hardware or software design with respect to its specification. Verification environments written in *e* provide a model of the environment in which the design is expected to function, including the kinds of erroneous conditions the design needs to withstand. A typical verification environment is capable of generating user-controlled test inputs with statistically interesting characteristics. Such an environment can check the validity of the design responses. Functional coverage metrics are used to control the verification effort and gauge the quality of the design. *e* verification environments can be used throughout the design cycle, from a high-level architectural model to a fully realized system. A definition of the *e* language syntax and semantics and how tool developers and verification engineers should use them are contained in this standard.

Keywords: assertion, concurrent programming, constraint, dynamic verification, functional coverage, functional verification, IEEE 1647™, simulation, temporal logic, test generation

The Institute of Electrical and Electronics Engineers, Inc.
3 Park Avenue, New York, NY 10016-5997, USA

Copyright © 2017 by The Institute of Electrical and Electronics Engineers, Inc.
All rights reserved. Published 6 January 2017. Printed in the United States of America.

IEEE and POSIX are registered trademarks in the U.S. Patent & Trademark Office, owned by The Institute of Electrical and Electronics Engineers, Incorporated.

Java is a trademark of Sun Microsystems, Inc. in the United States and other countries.

Perl is a registered trademark of Perl, Inc.

SystemC is a trademark of Accellera Systems Initiative Inc.

Verilog is a registered trademark of Cadence Design Systems, Inc.

Print: ISBN 978-1-5044-2139-3 STDPD20998
PDF: ISBN 978-1-5044-2138-6 STD20998

IEEE prohibits discrimination, harassment, and bullying.

For more information, visit <http://www.ieee.org/web/aboutus/whatis/policies/p9-26.html>.

No part of this publication may be reproduced in any form, in an electronic retrieval system or otherwise, without the prior written permission of the publisher.

Important Notices and Disclaimers Concerning IEEE Standards Documents

IEEE documents are made available for use subject to important notices and legal disclaimers. These notices and disclaimers, or a reference to this page, appear in all standards and may be found under the heading “Important Notice” or “Important Notices and Disclaimers Concerning IEEE Standards Documents.”

Notice and Disclaimer of Liability Concerning the Use of IEEE Standards Documents

IEEE Standards documents (standards, recommended practices, and guides), both full-use and trial-use, are developed within IEEE Societies and the Standards Coordinating Committees of the IEEE Standards Association (“IEEE-SA”) Standards Board. IEEE (“the Institute”) develops its standards through a consensus development process, approved by the American National Standards Institute (“ANSI”), which brings together volunteers representing varied viewpoints and interests to achieve the final product. Volunteers are not necessarily members of the Institute and participate without compensation from IEEE. While IEEE administers the process and establishes rules to promote fairness in the consensus development process, IEEE does not independently evaluate, test, or verify the accuracy of any of the information or the soundness of any judgments contained in its standards.

IEEE does not warrant or represent the accuracy or content of the material contained in its standards, and expressly disclaims all warranties (express, implied and statutory) not included in this or any other document relating to the standard, including, but not limited to, the warranties of: merchantability; fitness for a particular purpose; non-infringement; and quality, accuracy, effectiveness, currency, or completeness of material. In addition, IEEE disclaims any and all conditions relating to: results; and workmanlike effort. IEEE standards documents are supplied “AS IS” and “WITH ALL FAULTS.”

Use of an IEEE standard is wholly voluntary. The existence of an IEEE standard does not imply that there are no other ways to produce, test, measure, purchase, market, or provide other goods and services related to the scope of the IEEE standard. Furthermore, the viewpoint expressed at the time a standard is approved and issued is subject to change brought about through developments in the state of the art and comments received from users of the standard.

In publishing and making its standards available, IEEE is not suggesting or rendering professional or other services for, or on behalf of, any person or entity nor is IEEE undertaking to perform any duty owed by any other person or entity to another. Any person utilizing any IEEE Standards document, should rely upon his or her own independent judgment in the exercise of reasonable care in any given circumstances or, as appropriate, seek the advice of a competent professional in determining the appropriateness of a given IEEE standard.

IN NO EVENT SHALL IEEE BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO: PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE PUBLICATION, USE OF, OR RELIANCE UPON ANY STANDARD, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE AND REGARDLESS OF WHETHER SUCH DAMAGE WAS FORESEEABLE.

Translations

The IEEE consensus development process involves the review of documents in English only. In the event that an IEEE standard is translated, only the English version published by IEEE should be considered the approved IEEE standard.

Official statements

A statement, written or oral, that is not processed in accordance with the IEEE-SA Standards Board Operations Manual shall not be considered or inferred to be the official position of IEEE or any of its committees and shall not be considered to be, or be relied upon as, a formal position of IEEE. At lectures, symposia, seminars, or educational courses, an individual presenting information on IEEE standards shall make it clear that his or her views should be considered the personal views of that individual rather than the formal position of IEEE.

Comments on standards

Comments for revision of IEEE Standards documents are welcome from any interested party, regardless of membership affiliation with IEEE. However, IEEE does not provide consulting information or advice pertaining to IEEE Standards documents. Suggestions for changes in documents should be in the form of a proposed change of text, together with appropriate supporting comments. Since IEEE standards represent a consensus of concerned interests, it is important that any responses to comments and questions also receive the concurrence of a balance of interests. For this reason, IEEE and the members of its societies and Standards Coordinating Committees are not able to provide an instant response to comments or questions except in those cases where the matter has previously been addressed. For the same reason, IEEE does not respond to interpretation requests. Any person who would like to participate in revisions to an IEEE standard is welcome to join the relevant IEEE working group.

Comments on standards should be submitted to the following address:

Secretary, IEEE-SA Standards Board
445 Hoes Lane
Piscataway, NJ 08854 USA

Laws and regulations

Users of IEEE Standards documents should consult all applicable laws and regulations. Compliance with the provisions of any IEEE Standards document does not imply compliance to any applicable regulatory requirements. Implementers of the standard are responsible for observing or referring to the applicable regulatory requirements. IEEE does not, by the publication of its standards, intend to urge action that is not in compliance with applicable laws, and these documents may not be construed as doing so.

Copyrights

IEEE draft and approved standards are copyrighted by IEEE under U.S. and international copyright laws. They are made available by IEEE and are adopted for a wide variety of both public and private uses. These include both use, by reference, in laws and regulations, and use in private self-regulation, standardization, and the promotion of engineering practices and methods. By making these documents available for use and adoption by public authorities and private users, IEEE does not waive any rights in copyright to the documents.

Photocopies

Subject to payment of the appropriate fee, IEEE will grant users a limited, non-exclusive license to photocopy portions of any individual standard for company or organizational internal use or individual, non-commercial use only. To arrange for payment of licensing fees, please contact Copyright Clearance Center, Customer Service, 222 Rosewood Drive, Danvers, MA 01923 USA; +1 978 750 8400. Permission to photocopy portions of any individual standard for educational classroom use can also be obtained through the Copyright Clearance Center.

Updating of IEEE Standards documents

Users of IEEE Standards documents should be aware that these documents may be superseded at any time by the issuance of new editions or may be amended from time to time through the issuance of amendments, corrigenda, or errata. An official IEEE document at any point in time consists of the current edition of the document together with any amendments, corrigenda, or errata then in effect.

Every IEEE standard is subjected to review at least every ten years. When a document is more than ten years old and has not undergone a revision process, it is reasonable to conclude that its contents, although still of some value, do not wholly reflect the present state of the art. Users are cautioned to check to determine that they have the latest edition of any IEEE standard.

In order to determine whether a given document is the current edition and whether it has been amended through the issuance of amendments, corrigenda, or errata, visit the IEEE-SA Website at <http://ieeexplore.ieee.org/> or contact IEEE at the address listed previously. For more information about the IEEE-SA or IEEE's standards development process, visit the IEEE-SA Website at <http://standards.ieee.org>.

Errata

Errata, if any, for all IEEE standards can be accessed on the IEEE-SA Website at the following URL: <http://standards.ieee.org/findstds/errata/index.html>. Users are encouraged to check this URL for errata periodically.

Patents

Attention is called to the possibility that implementation of this standard may require use of subject matter covered by patent rights. By publication of this standard, no position is taken by the IEEE with respect to the existence or validity of any patent rights in connection therewith. If a patent holder or patent applicant has filed a statement of assurance via an Accepted Letter of Assurance, then the statement is listed on the IEEE-SA Website at <http://standards.ieee.org/about/sasb/patcom/patents.html>. Letters of Assurance may indicate whether the Submitter is willing or unwilling to grant licenses under patent rights without compensation or under reasonable rates, with reasonable terms and conditions that are demonstrably free of any unfair discrimination to applicants desiring to obtain such licenses.

Essential Patent Claims may exist for which a Letter of Assurance has not been received. The IEEE is not responsible for identifying Essential Patent Claims for which a license may be required, for conducting inquiries into the legal validity or scope of Patents Claims, or determining whether any licensing terms or conditions provided in connection with submission of a Letter of Assurance, if any, or in any licensing agreements are reasonable or non-discriminatory. Users of this standard are expressly advised that determination of the validity of any patent rights, and the risk of infringement of such rights, is entirely their own responsibility. Further information may be obtained from the IEEE Standards Association.

Participants

At the time this standard was submitted to the IEEE-SA Standards Board for approval, the IEEE *e* Functional Verification Language (*e*WG) Working Group had the following members and observers:

Darren Galpin, *Chair*
Srinivasan Venkataramanan, *Vice Chair*
Alan Perlman, Karen Ochoa, Amy Witherow, *Technical Editors*

Cristian Amitroaie
Mike Bartley
Erez Bashi
Stefan Birman
Hannes Froehlich
Kishore Karnane

Yaron Kashi
Silas McDermott
Genadi Osowiecki
Andrew Piziali
Aleksandar Randjic
Scott Roland
Damian Savage

Uwe Simm
Akash Singh
Marat Teplitsky
Yuri Tsoglin
Matan Vax
Greg White

The following members of the individual balloting committee voted on this standard. Balloters may have voted for approval, disapproval, or abstention.

Sourav Dutta
Hannes Froehlich
Darren Galpin
Randall Groves
Werner Hoelzl
Noriyuki Ikeuchi

Adri Jovin
Piotr Karocki
Yaron Kashi
Adam Ley
Nick S.A. Nikjoo
Bansi Patel
Andrew Piziali

Iulian Profir
Robert Robinson
Walter Struppler
Richard Thayer
John Vergis
Paul Work

When the IEEE-SA Standards Board approved this standard on 30 June 2016, it had the following membership:

Jean-Philippe Faure, *Chair*
Ted Burse, *Vice Chair*
John D. Kulick, *Past Chair*
Konstantinos Karachalios, *Secretary*

Chuck Adams
Masayuki Ariyoshi
Stephen Dukes
Jianbin Fan
Ronald W. Hotchkiss
J. Travis Griffith

Gary Hoffman
Michael Janezic
Joseph L. Koepfinger*
Hung Ling
Kevin Lu
Gary Robinson
Annette D. Reilly

Mehmet Ulema
Yingli Wen
Howard Wolfman
Don Wright
Yu Yuan
Daidi Zhong

*Member Emeritus

Introduction

This introduction is not part of IEEE Std 1647™-2016, IEEE Standard for the Functional Verification Language *e*.

The *e functional verification language* is an application-specific programming language aimed at the problem of verifying functional correctness of hardware and software designs. Simply stated, functional verification attempts to provide a quantitative answer to the question: How well does the design match the functional specification?

Functional correctness of chip designs grew in criticality from the mid-1980s. As design complexity kept growing, ad hoc testing methods ran out of steam and a more systematic verification approach was necessary. Manually constructed test suites, the early method of choice, became both uneconomical and ineffective when scaled up. As a result, many companies supplemented manual test suites with *pseudo-random generation* of input stimulus. Such test generation programs were typically built for a particular project or a particular architecture. They turned out to be expensive to develop and maintain, but once functional, they would clean up the design in a very thorough way.

A key observation made by Yoav Hollander, the creator of *e*, was that verification environments of different projects have a lot in common and yet each verification environment is structured to match a particular design specification. Hollander's solution was to create a language that had verification-specific constructs as primitives and the full capabilities of a high-level language for customization. In particular, pseudo-random test generation became a built-in capability of the language. Early prototypes of the language were experimented with as early as 1993, showing significant productivity gains.

The *e* language was productized by Verisity, Ltd., in 1996, as part of a functional verification tool suite. The proliferation of the *e* language and the growing investment in *e*-based intellectual property (IP) compelled the creation of the *e steering committee* in June of 2002, composed of individuals from Texas Instruments, Rambus, ST Microelectronics, Cisco, Intel, Axis System, STARC, and Verisity. The *e steering committee* recommended the *e* language be standardized through The Institute of Electrical and Electronics Engineers (IEEE). Accepting the recommendation, Verisity released the rights to the language to the IEEE in June of 2003.

The *e* language, in its current form, brings together concepts from many domains.

- *e* has a basic object-oriented (OO) programming model, with implicit memory management and single inheritance. In this, *e* is similar to Java™.¹
- Beyond objects, *e* supports *aspects*, which can be viewed as layers cutting across multiple objects. Adding an aspect to an existing program refines the program by introducing a coherent change to a plurality of objects.
- *e* supports constraints as object features. Constraints are used to refine object modeling. The execution model of the language involves resolving constraint systems and picking random values that would satisfy constraint systems.
- *e* is a strongly typed language, like Pascal and Modula.
- *e* has concurrency constructs and modeling blocks for hierarchical composition, similar to hardware description languages like Verilog® (see IEEE Std 1364™) and VHDL (see IEC/IEEE 61691-1-1).^{1,2} Concurrency in *e* is synchronous, like in Esterel.

¹Java is a trademark of Sun Microsystems, Inc. in the United States and other countries. Verilog is a registered trademark of Cadence Design Systems, Inc. This information is given for the convenience of users of this standard and does not constitute an endorsement by the IEEE of these products. Equivalent products may be used if they can be shown to lead to the same results.

²Information on references can be found in [Clause 2](#).

- *e* contains a temporal language that borrows from Linear Temporal Logic and Interval Temporal Logic.
- *e* has many built-in constructs aimed at simplifying common programming tasks; built-in support for lists and hashes; and pattern matching and string- and file-manipulation features, which are borrowed from PerlTM.³
- The *e* syntax is extendable with a powerful macro capability.

This combination of concepts caters directly to the needs of verification engineers, removing the need to cobble together multiple components in different languages.

As with any programming language, the source of ingenuity is with the programmer. Verification engineers need sound methodologies, creativity, an inquisitive mind, and a keen eye for poorly specified aspects. Yet experience with *e* shows that when put to good use, the *e* language fosters productivity and quality results.

³Perl is a registered trademark of Perl, Inc. This information is given for the convenience of users of this standard and does not constitute an endorsement by the IEEE of these products. Equivalent products may be used if they can be shown to lead to the same results.

Contents

1.	Overview.....	15
1.1	Scope.....	15
1.2	Purpose.....	15
1.3	Verification environments	15
1.4	Basic concepts relating to this standard	16
1.5	Conventions used.....	22
1.6	Use of color in this standard	23
1.7	Contents of this standard.....	24
2.	Normative references	26
3.	Definitions, acronyms, and abbreviations.....	26
3.1	Definitions	26
3.2	Acronyms and abbreviations	28
4.	<i>e</i> basics.....	30
4.1	Lexical conventions	30
4.2	Syntactic elements	37
4.3	Struct hierarchy and name resolution	43
4.4	Ranges.....	49
4.5	Operator precedence	50
4.6	Evaluation order of expressions.....	51
4.7	Bitwise operators	51
4.8	Boolean operators	53
4.9	Arithmetic operators	55
4.10	Comparison operators.....	56
4.11	String matching.....	60
4.12	Extraction and concatenation operators.....	62
4.13	Scalar modifiers	66
4.14	Parentheses.....	67
4.15	list.method()	67
4.16	Special-purpose operators.....	68
5.	Data types	72
5.1	<i>e</i> data types.....	72
5.2	Untyped expressions	78
5.3	Assignment rules.....	79
5.4	Real data type.....	82
5.5	Precision rules for numeric operations	84
5.6	Automatic type casting	86
5.7	Defining and extending scalar types.....	87
5.8	Type-related constructs.....	90
6.	Structs, subtypes, and fields.....	97
6.1	Structs overview	97
6.2	Defining structs: struct	98

6.3	Extending structs: extend type	99
6.4	Restrictions on inheritance	99
6.5	Extending subtypes	100
6.6	Creating subtypes with when	100
6.7	Extending when subtypes	102
6.8	Defining fields: field	103
6.9	Defining list fields	105
6.10	Projecting list of fields	107
6.11	Defining attribute fields	107
7.	Units	109
7.1	Overview	109
7.2	Defining units and fields of type unit	112
7.3	Unit attributes	115
7.4	Predefined methods of any_unit	116
7.5	Unit-related predefined methods of any_struct	118
7.6	Unit-related predefined routines	120
8.	Template types	122
8.1	Defining a template type	122
8.2	Extending a template	125
8.3	Instantiating a template type	126
8.4	Template subtype instances	127
9.	<i>e</i> ports	129
9.1	Introduction to <i>e</i> ports	129
9.2	Using simple ports	130
9.3	Using buffer ports	132
9.4	Using event ports	133
9.5	Using method ports	134
9.6	Defining and referencing ports	136
9.7	Port attributes	144
9.8	Buffer port methods	156
9.9	MVL methods for simple ports	158
9.10	Global MVL routines	169
9.11	Comparative analysis of ports and tick access	173
9.12	<i>e</i> port binding	174
9.13	Transaction level modeling interface ports in <i>e</i>	175
9.14	TLM Sockets in <i>e</i>	184
10.	Constraints and generation	191
10.1	Types of constraints	191
10.2	Generation concepts	191
10.3	Type constraints	209
10.4	Defining constraints	212
10.5	Invoking generation	217

11.	Temporal struct members	220
11.1	Events.....	220
11.2	on	224
11.3	on event-port	225
11.4	expect assume	226
11.5	Procedural API for temporal operators on event and expect struct members	227
12.	Temporal expressions	241
12.1	Overview.....	241
12.2	Temporal operators and constructs	244
12.3	Success and failure of a temporal expression	259
13.	Time-consuming actions.....	261
13.1	Synchronization actions	261
13.2	Concurrency actions	263
13.3	State machines	264
14.	Coverage constructs.....	269
14.1	Defining coverage groups: cover	269
14.2	Defining basic coverage items: item	272
14.3	Defining cross coverage items: cross	277
14.4	Defining transition coverage items: transition	279
14.5	Extending coverage groups: cover ... using also ... is also	281
14.6	Extending coverage items: item ... using also	282
14.7	Coverage API.....	282
14.8	Coverage methods for the covers struct.....	288
15.	Macros	294
15.1	Overview.....	294
15.2	define-as statement	295
15.3	define-as-computed statement	295
15.4	Match expression structure	296
15.5	Interpretation of match expressions.....	298
15.6	Macro expansion code	299
16.	Print, checks, and error handling	302
16.1	print	302
16.2	Handling DUT errors	302
16.3	Handling user errors.....	308
16.4	Handling programming errors: assert	310
17.	Methods	311
17.1	Rules for defining and extending methods	311
17.2	Invoking methods	318
17.3	Parameter passing	323
17.4	Using the C interface	325

18.	Creating and modifying <i>e</i> variables	327
18.1	About <i>e</i> variables	327
18.2	var	327
18.3	=	328
18.4	op=	328
18.5	<=	329
19.	Packing and unpacking	331
19.1	Basic packing	331
19.2	Predefined pack options	334
19.3	Customizing pack options	335
19.4	Packing and unpacking specific types	335
19.5	Implicit packing and unpacking	341
20.	Control flow actions	342
20.1	Conditional actions	342
20.2	Iterative actions	344
20.3	File iteration actions	349
20.4	Actions for controlling the program flow	350
21.	Importing and preprocessor directives	352
21.1	Importing <i>e</i> modules	352
21.2	#ifdef, #ifndef	353
21.3	#define	354
21.4	#undef	355
22.	Encapsulation constructs	356
22.1	package: package-name	356
22.2	package: type-declaration	356
22.3	package protected private: struct-member	357
22.4	Scope operator (::)	358
23.	Simulation-related constructs	359
23.1	force	359
23.2	release	359
23.3	Tick access: 'hdl-pathname'	360
24.	Messages	361
24.1	Overview	361
24.2	Message model	361
24.3	Message execution	361
24.4	Structured debug messages	362
24.5	message and messagef	368
24.6	Tag	368
24.7	Verbosity	369
24.8	Predefined type sdm_handler	369
24.9	Messages Interface	371

25.	Sequences.....	393
25.1	Overview.....	393
25.2	Sequence statement	395
25.3	do sequence action	397
25.4	Sequence struct types and members	398
25.5	BFM-driver-sequence flow diagrams	403
26.	List pseudo-methods library	407
26.1	Pseudo-methods overview	407
26.2	Using list pseudo-methods	407
26.3	Pseudo-methods to modify lists	407
26.4	General list pseudo-methods.....	416
26.5	Math and logic pseudo-methods	431
26.6	List CRC pseudo-methods	434
26.7	Keyed list pseudo-methods	436
27.	Predefined methods library	439
27.1	Predefined methods of sys	439
27.2	Predefined methods of any_struct.....	439
27.3	Methods and predefined attributes of unit any_unit	442
27.4	Set Pseudo-methods	443
27.5	Other pseudo-methods	450
27.6	Coverage methods.....	452
28.	Predefined routines library.....	453
28.1	Deep copy and compare routines.....	453
28.2	Integer arithmetic routines	456
28.3	Real arithmetic routines	460
28.4	bitwise_op()	461
28.5	get_all_units()	462
28.6	String routines.....	462
28.7	Output routines	470
28.8	Operating system interface routines	472
28.9	set_config()	476
28.10	Random routines	476
28.11	Simulation-related routines	476
29.	Predefined file routines library	479
29.1	File names and search paths.....	479
29.2	File handles	479
29.3	Low-level file methods	479
29.4	General file routines.....	484
29.5	Reading and writing structs	490
30.	Reflection API	493
30.1	Introduction.....	493
30.2	Type information	494
30.3	Aspect information	509

30.4	Value query and manipulation	515
31.	Predefined resource sharing control structs	520
31.1	Semaphore methods	520
31.2	How to use the semaphore struct	521
32.	Intellectual property protection.....	525
32.1	Encryption.....	525
32.2	Decryption	525
32.3	Reflection API	526
32.4	Encryption targets	526
	Annex A (informative) Bibliography	527
	Annex B (normative) Source code serialization	528
	Annex C (informative) Comparison of when and like inheritance.....	536
	Annex D (normative) Name spaces	544
	Annex E (informative) Reflection API examples.....	552
	Annex F (informative) Encryption targets.....	556

IEEE Standard for the Functional Verification Language *e*

IMPORTANT NOTICE: *IEEE Standards documents are not intended to ensure safety, health, or environmental protection, or ensure against interference with or from other devices or networks. Implementers of IEEE Standards documents are responsible for determining and complying with all appropriate safety, security, environmental, health, and interference protection practices and all applicable laws and regulations.*

This IEEE document is made available for use subject to important notices and legal disclaimers. These notices and disclaimers appear in all publications containing this document and may be found under the heading “Important Notice” or “Important Notices and Disclaimers Concerning IEEE Documents.” They can also be obtained on request from IEEE or viewed at <http://standards.ieee.org/IPR/disclaimers.html>.

1. Overview

This clause explains the scope and purpose of this standard; gives an overview of the basic concepts, major semantic components, and conventions used in this standard; and summarizes its contents.

1.1 Scope

This standard defines the *e* functional verification language. This standard aims to serve as an authoritative source for the definition of (a) syntax and semantics of *e* language constructs, (b) the *e* language interaction with standard simulation languages, and (c) *e* language libraries.

1.2 Purpose

This standard serves the community involved with functional verification of electronic designs using the *e* language. It provides an implementation-independent definition of the *e* language and facilitates the development of *e* language based design automation tools.

1.3 Verification environments

Electronic systems are integrated circuits (ICs), boards, or modules combining multiple ICs together, along with optional embedded processors and software components. Electronic systems are built to *specifications* that anticipate the environment in which such systems are expected to function and define the expected system functionality. *Functional verification* measures how well a system meets its specification. Even with moderately complex systems this question cannot be answered by inspection. For all modern electronic systems, a sophisticated *verification process* needs to accompany the design process to ensure compliance with the specification.