

IEEE Standard for Access and Control of Instrumentation Embedded within a Semiconductor Device

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IEEE Standard for Access and Control of Instrumentation Embedded within a Semiconductor Device

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Test Technology Standards Committee
of the
IEEE Computer Society

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Abstract: A methodology for accessing instrumentation embedded within a semiconductor device, without defining the instruments or their features themselves, via the IEEE 1149.1™ test access port (TAP) and/or other signals, is described in this standard. The elements of the methodology include a hardware architecture for the on-chip network connecting the instruments to the chip pins, a hardware description language to describe this network, and a software language and protocol for communicating with the instruments via this network.

Keywords: access network, built-in self-test (BIST), boundary scan, debug, design for testability (DFT), embedded instruments, IEEE 1149.1™, IEEE 1687™, Instrument Connectivity Language (ICL), internal JTAG (IJTAG), Joint Test Action Group (JTAG), on-chip instrumentation, Procedural Description Language (PDL), test, Tool Command Language (Tcl)

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Introduction

This introduction is not part of IEEE Std 1687™-2014, IEEE Standard for Access and Control of Instrumentation Embedded within a Semiconductor Device.

The development of this standard stemmed from two independent (and unaware of each other) efforts at the 2004 International Test Conference to address issues surrounding the use of the IEEE 1149.1 test access port (TAP) for purposes well beyond boundary scan testing. These efforts were merged, and the Internal JTAG (IJTAG) Working Group was born. The scope of the effort was refined in the following months as more members joined the group to focus on the access to design for testability (DFT) features (more generally called *instruments*) inside devices. The development of the ideas comprising this standard can be traced by presentations at a series of conferences, workshops, and symposia, including ITC'05, BAST'06, ITSW'06, VTS'06, ETS'06, ITC'06, VTS'07, ETS'07, ITC'07, ETS'08, ITC'08, and IOLTS'09, ITC'11, ETS'12, ITC'12, and ITC'13.

Frequently asked questions

The IEEE 1687 web site will include an FAQ.^a

^aSee <http://grouper.ieee.org/groups/1687/>.

Contents

1. Overview	1
1.1 Scope	1
1.2 Purpose	1
1.3 Background.....	2
1.4 Organization	2
1.5 Context	3
2. Normative references.....	4
3. Definitions, acronyms, and abbreviations	4
3.1 Definitions	4
3.2 Acronyms and abbreviations	10
4. Technology	11
4.1 Introduction	11
4.2 Serial access networks	11
4.3 On-chip instruments	18
5. Hardware architecture	19
5.1 Introduction to the IEEE 1687 network.....	19
5.2 Hierarchical IEEE 1687 networks	19
5.3 Controller.....	22
5.4 Instrument interface.....	22
5.5 Access network.....	23
5.6 Test data register.....	30
5.7 Local reset	34
5.8 Delivery and integration of instruments	38
5.9 Embedded TAP controller	39
5.10 Definitions of the structure of IEEE 1687 hardware architecture.....	44
5.11 Port functions of a module.....	45
5.12 Signals between and within IEEE 1687 modules	47
5.13 Components comprising a module	48
5.14 TAP finite state machine embedded in an IEEE 1687 module	50
5.15 Access network behavior	53
5.16 Plug-and-play interfaces	53
6. Instrument Connectivity Language (ICL)	56
6.1 ICL introduction	56
6.2 ICL overview	57
6.3 ICL lexical conventions and definitions	59
6.4 ICL primitive element keywords and statements.....	73
6.5 ICL informational statements	135
6.6 ICL connectivity	141
6.7 Inferring information in implicit ICL	141
6.8 Active values for control signals	142
7. Procedural Description Language (PDL): level-0	143
7.1 Purpose	143
7.2 PDL levels	143
7.3 Basic PDL concepts.....	144
7.4 Retargeting of PDL.....	147

7.5 PDL level-0 overview	149
7.6 PDL general rules	152
7.7 Generic PDL tokens.....	154
7.8 PDL numbers.....	155
7.9 PDL level-0 commands	157
8. Procedural Description Language: level-1 (Tcl)	182
8.1 Purpose	182
8.2 Tcl command extensions	182
8.3 PDL level-1 overview.....	183
8.4 PDL level-1 commands	183
8.5 PDL level-1 example.....	189
Annex A (informative) ICL grammar.....	190
Annex B (informative) PDL level-0 grammar.....	199
Annex C (informative) PDL level-1 grammar.....	203
Annex D (informative) PDL differences between IEEE Std 1687-2014 and IEEE Std 1149.1-2013	204
Annex E (informative) Examples	212
Annex F (informative) Design guidance	255
Annex G (informative) Bibliography	267

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1. Overview

1.1 Scope

This standard develops a methodology for access to embedded instrumentation, without defining the instruments or their features themselves, via the IEEE 1149.1™ test access port (TAP) and additional signals that may be required. The elements of the methodology include a description language for the characteristics of the features and for communication with the features, and requirements for interfacing to the features.

1.2 Purpose

IEEE Std 1149.1 specifies circuits to be embedded within a semiconductor device to support board test; namely, the TAP, TAP Controller, and a number of internal registers.¹ In practice the TAP and TAP Controller are being used for other functions well beyond boundary scan in an ad-hoc manner across the industry to access a wide variety of embedded instruments. The purpose of the IEEE 1687 initiative is to provide an extension to IEEE Std 1149.1 specifically aimed at using the TAP to manage the configuration, operation, and collection of data from this embedded instrumentation circuitry.

¹ Information on references can be found in Clause 2.