1394™

IEEE Standard for a High-Performance Serial Bus

IEEE Computer Society

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Microprocessor Standards Committee

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Abstract: This standard provides specifications for a high-speed serial bus that supports both asynchronous and isochronous communication and integrates well with most IEEE standard 32-bit and 64-bit parallel buses. It is intended to provide a low-cost interconnect between cards on the same backplane, cards on other backplanes, and external peripherals. Interfaces to longer distance transmission media [such as unshielded twisted pair (UTP), optical fiber, and plastic optical fiber (POF)] allow the interconnection to be extended throughout a local network. This standard follows the command and status register (CSR) architecture of IEEE Std 1212™-2001.
Keywords: asynchronous, bus, computers, high-speed serial bus, interconnect, isochronous, optical fiber, plastic optical fiber, POF, unshielded twisted pair, UTP

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Introduction

This introduction is not part of IEEE Std 1394-2008, IEEE Standard for a High-Performance Serial Bus.

The IEEE 1394 base standard was issued in 1995, followed by three amendments: IEEE Std 1394a™-2000, IEEE Std 1394b™-2002, and IEEE Std 1394c™-2006. In December 2002, a project was approved to merge the first two amendments into the base standard. Work on this project did not begin until July 2006. The project authorization was extended for two years and expanded to include IEEE Std 1394c-2006 as well as a large number of errata and corrigenda and several new features that had been developed over the intervening years. Editorial work on the standard was completed in April 2008.

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1. Overview

1.1 Scope and purpose

1.1.1 Scope

This standard describes a high-speed, low-cost serial bus suitable for use as a peripheral bus, a backup to parallel backplane buses, or a local area network. Highlights of the serial bus include the following:

a) Bus transactions that include both block and single quadlet reads and writes, as well as an “isochronous” mode that provides a low-overhead guaranteed bandwidth service.

b) A fair bus access mechanism that guarantees all nodes equal access. The backplane environment adds a priority mechanism, but one that ensures that nodes using the fair protocol are still guaranteed at least partial access.

c) Automatic assignment of node addresses—no need for address switches.

d) A physical layer (PHY) supporting both long-haul and short-haul cable media and backplane buses.

e) Variable speed data transmission based on ISDN-compatible[1] bit rates from 24.576 Mbit/s for transistor-transistor logic (TTL) backplanes to 49.152 Mbit/s for backplane transceiver logic (BTL) backplanes. For the cable medium, data transmission rates of 98.304 Mbit/s (known as S100), S200, S400, S800, S1600, and S3200 are supported.

f) A short-haul cable medium that allows up to 16 physical connections (cable hops), each up to 4.5 m, giving a total cable distance of 72 m between any two devices. Bus management recognizes smaller configurations to optimize performance.

[1]The lowest data rate of 24.576 Mbit/s is exactly 18 times the 1.536 Mbit/s and 12 times the 2.048 Mbit/s Integrated Services Digital Network (ISDN) primary rates. It is also an integer multiple of the ISDN basic rate and numerous other communication rates.

g) A long-haul cable medium that permits connections up to 100 m in length over unshielded twisted pair (UTP) cable and glass optical fiber (GOF) and up to 50 m over plastic optical fiber (POF).

h) Consistency with ISO/IEC 13213:1994 (IEEE Std 1212™, 1994 Edition).[2]

1.1.2 Purpose

This standard incorporates the contents of IEEE Std 1394™-1995 as revised by IEEE Std 1394a™-2000, IEEE Std 1394b™-2002, and IEEE Std 1394c™-2006. In addition, over 100 errata have been corrected, and several new features have been added per Q.12.

1.2 Document organization

This standard contains this overview, a list of definitions, an informative summary description, chapters of technical specification, and application annexes. The new reader should read the document in order. The actual specification follows the summary and is organized from the bottom up; that is, the specification starts at the PHY (cable and backplane), works up to the link layer, the transaction layer, and the bus management layer.

1.3 Serial bus applications

Three primary applications have driven the design and architecture of the serial bus: an alternate for a parallel backplane bus, a low-cost peripheral bus, and a bus bridge between architecturally compatible 32-bit buses.

1.3.1 Alternate bus

There are five main reasons for providing a serial bus on a system that already has a parallel bus:

a) The many modules that make up a system might operate on different backplane bus standards, yet they need to work together.

b) Although located within the same enclosure, a system is too large or physically disperse to use a single backplane, yet modules in the different backplanes have to communicate.

c) One or more modules of a system are located neither on the same backplane nor within the same enclosure.

d) A redundant data path increases fault tolerance. A system can use the serial bus to isolate and diagnose errors without depending on the failed parallel bus.

e) Many system modules are price-sensitive and do not need the full bandwidth of a parallel bus.

1.3.2 Low-cost peripheral bus

The serial bus can also be used as a powerful and low-cost peripheral interconnect. The compact serial bus cable and connector allow bandwidths comparable with existing input/output (I/O) interconnect standards. The serial bus has the added advantage of architectural compatibility with parallel computer buses; this compatibility leads to lower communications overhead than with limited, function-dedicated I/O interconnects.

[2]Information on references can be found in Clause 2.

1.3.3 Bus bridge

The serial bus architecture limits the number of nodes on any bus to 63, but supports multiple bus systems via bus bridges. The command and status register (CSR) architecture defines the serial bus addressing structure, which allows almost 2^{16} nodes.

A bus bridge normally eavesdrops on the bus, ignoring all transactions between local addresses but listening carefully for remote transactions. When the bridge receives a packet for a remote address, it forwards the packet to an adjacent bus.

Although the serial bus may be used in many bus configurations, when used to bridge CSR-architecture-compliant buses, it is expected to be used mostly in a hierarchical bus fashion, as illustrated in Figure 1-1 (where bus #5 is a serial bus and bridges together other CSR-architecture-compliant bus #1 through bus #4, bus #1 could be IEEE 896 Futurebus+® ([B23], [B24], [B26]),[3,4] bus #2 could be IEEE 1596 scalable coherent interface (SCI) ([B25]), and so on).

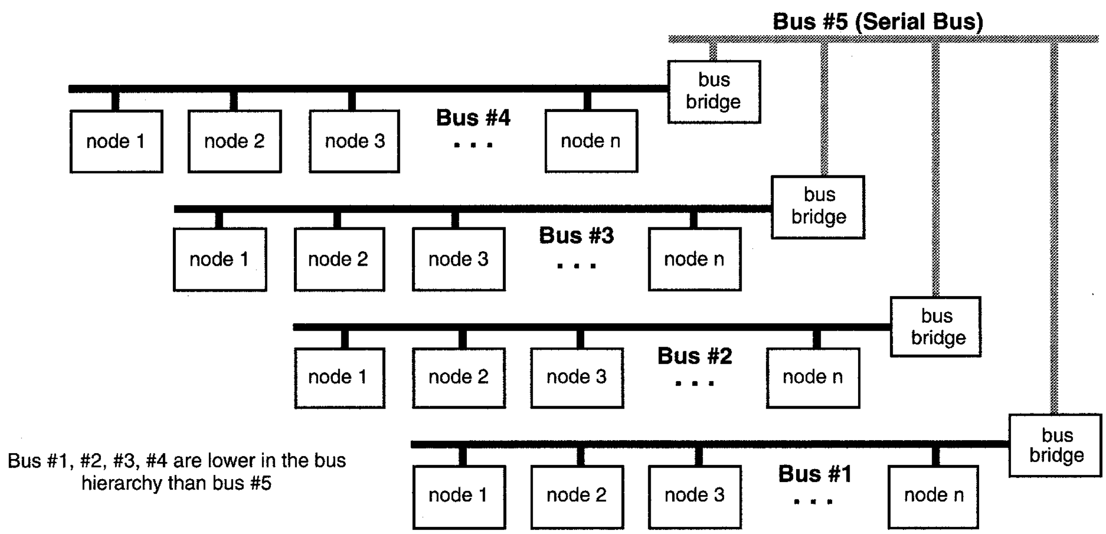

Figure 1-1—Example hierarchical bus topology

1.4 Service model

This standard uses a protocol model with multiple layers. Each layer provides services to the next higher layer and to serial bus management (SBM). These services are abstractions of a possible implementation; an actual implementation may be significantly different and still meet all the requirements. The method by which these services are communicated between the layers is not defined by this standard. Four types of service are defined by this standard as follows:

a) *Request service.* A request service is a communication from a layer to a lower or adjacent layer to request some action. A request may also communicate parameters that may or may not be associated with an action. A request may or may not be confirmed. A data transfer request usually triggers a corresponding indication on peer node(s). (Because broadcast addressing is supported on a serial bus, it is possible for the request to trigger a corresponding indication on multiple nodes.)

[3]Futurebus+ is a registered trademark of the Institute of Electrical and Electronics Engineers, Inc.
[4]The numbers in brackets correspond to the numbers of the bibliography in Annex S.